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**A COMPARATIVE STUDY OF ELECTRIC POWER  
DISTRIBUTION SYSTEMS FOR SPACECRAFT**

**Final Report for the Period  
June 19, 1989 to December 31, 1989**

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## FOREWORD

This report presents the results of NASA Grant NAG 3-708, "A Comparative Study of Electric Power Distribution Systems for Spacecraft," for the period of June 19, 1989 to December 31, 1989. This research was performed by the University of Toledo for the NASA Lewis Research Center.



## TABLE OF CONTENTS

I. INTRODUCTION.....	1
II. AC vs. DC DISTRIBUTION.....	2
Introduction.....	2
Power Levels and Types of Sources.....	3
High Voltage DC.....	4
High Voltage AC.....	6
Summary.....	18
III. ANALYSIS OF NON-RESONANT TOPOLOGIES.....	21
INTRODUCTION.....	21
BUCK CONVERTER.....	22
Full-Bridge Buck Converter.....	25
Phase-Shift Gating.....	32
Half-Bridge Buck Converter.....	32
Push-Pull Buck Converter.....	36
Comparison of Buck Topologies.....	38
BOOST CONVERTER.....	42
Full-Bridge Boost Converter.....	45
OTHER DC-DC CONVERTERS.....	50
Weinberg Converter.....	50
TRW Converter.....	54
SUMMARY OF SUGGESTED DESIGNS.....	57
IV. ANALYSIS OF RESONANT TOPOLOGIES.....	60
SERIES-RESONANT INVERTER/CONVERTER.....	60
Variable-Frequency SRC Design and Performance.....	64

Fixed-Frequency SRC Design and Performance.....	73
SRC Interfacing Capacitors and Transformer.....	80
PARALLEL-LOADED RESONANT INVERTER/CONVERTER.....	87
Variable-Frequency PRC.....	88
Phase-Controlled PRI.....	97
PC-PRI with Rectifier Load.....	104
Pulse-Width-Controlled PRI.....	105
TRW Resonant Inverter.....	107
V. COMPARATIVE STUDIES.....	112
DC-DC CONVERTERS.....	112
DC-AC INVERTERS.....	114
Comparison of Four Topologies.....	114
Additional Topologies.....	121
Additional Considerations.....	122
Recommendations.....	124
VI. SUMMARY.....	126
VII. REFERENCES.....	128

## I. INTRODUCTION

This comparative study of electric power distribution systems for spacecraft concentrates on two interrelated issues: (1) the choice between dc and high-frequency ac, and (2) the converter/inverter topology to be used at the power source. The report opens first with a discussion of the relative merits of dc and ac distribution. Then, specific converter and inverter topologies are identified and analyzed in detail for the purpose of detailed comparison. Finally, specific topologies are recommended for use in dc and ac systems.

## II. AC vs. DC Distribution

### Introduction

Because of increasing electric power requirements for future spacecraft, it is becoming increasingly evident that alternatives to traditional 28 Vdc and 400 Hz ac distribution should be considered. Obvious reasons for this include the high cable weight of 28 Vdc and the high transformer and filter weights of 400 Hz. Two proposals that have received considerable attention are to simply use a higher dc voltage, such as 270 Vdc [16,17], or use a higher ac frequency, such as 20 kHz [1,2,6-15,18]. Both approaches have their pros and cons, but considerable debate has arisen as to what the relative merits are. As an example, it is sometimes argued that a 20 kHz system has the advantages of high efficiency and low weight, implying that high voltage dc does not enjoy these characteristics. Such a conclusion is incorrect since high efficiency is basically achieved by raising the voltage, and low weight is achieved by raising the voltage and the switching frequency. Thus 400 Hz will indeed be heavier than 20 kHz, but it should be capable of at least the same efficiency at the same voltage level. Likewise, a dc system should be capable of about the same efficiency as either 20 kHz or 400 Hz at the same voltage. Since dc/dc converters can switch at frequencies well above 20 kHz, dc may be capable of power/weight ratios that are actually higher than those for 20 kHz ac.

In light of the wide variety of possible systems and topologies, there is a need to collect the pertinent information and present it in a comparative format. This present study compares some of the more important characteristics of dc and higher-frequency ac and presents several different ways of implementation. For example, at least three methods have been proposed for implementing 20 kHz [2,6,18], and numerous converter topologies can be used to implement DC.



## **Power Levels and Types of Sources**

Because of the broad range of power levels and variety of proposed sources, it is unlikely that any one distribution system will be optimum for all possibilities. To provide a basis of comparison, this study will assume a load in the range of 100 kW, since this power level is one that has been proposed for future applications. To provide a frame of reference for the voltage, it will be assumed that distribution voltages will be in the range of 400-500 volts. This should allow reasonable cable sizes with currents in the 200-250 amp range. This voltage also allows the use of conventional converter designs using readily available semiconductors.

Regardless of the form of generation, all of the proposed high voltage dc and 20 kHz systems require input power from a dc source. For power levels in the range of 100 kW, the energy source will probably be a nuclear reactor. A few possibilities for deriving a dc voltage from the heat of the reactor are listed below:

1. Thermionic converter
2. Thermoelectric converter
3. Engine-driven alternator with rectification

The thermionic and thermoelectric converters are characterized by low voltage outputs in the 100 Vdc range, which is usually too low for distribution. Rectified alternators can operate at high voltages, however, and should not require any voltage boost.

Presumably, both high voltage dc and 20 kHz systems will be derived from some type of bridge converter with an output transformer. Therefore, either type should be able to work from a low or high voltage source, but there are at least two cases that tend to favor either DC or a two-stage AC system with a DC link. One case would be where the reactor is at a remote location from the spacecraft. If a low voltage source such as a thermoelectric is also used, there is some advantage in locating the electronic converter near the reactor to reduce the weight of the transmission cable to the spacecraft. DC transmission allows a simplified cable for this link and this tends to favor a dc system or a two stage ac system which uses a dc link. Another case

that might favor dc is the rectified alternator. If the alternator voltage is high enough and can be regulated, it may be possible to eliminate the source converter.

### **High Voltage DC**

A simple block diagram of a dc distribution system is shown in Fig. 2.1. This system offers certain advantages, some of which would be low EMI, simple cables, and the possible use of relatively simple magnetic blowout circuit breakers [3]. The most obvious drawback of dc compared to ac is that a converter is required for voltage scaling at the loads instead of a transformer. This factor becomes especially important at high distribution voltages or where there are several unregulated loads that require different voltages. If the power level is high enough, electro-mechanical circuit breakers may become a problem, but according to [3], this limitation is actually more serious for 20 kHz systems.

As with any system, it is absolutely necessary to use fault-tolerant converters. This term implies a converter that can operate in a current limit mode without damage if a short circuit occurs. A converter of this type will limit the current that must be interrupted by a DC breaker, and it can even be turned off momentarily to allow the breaker to open at no load (sometimes called "blinking"). Incidentally, while blinking can be used to decrease the stress on circuit breakers, it seems risky to totally depend on this, meaning all breakers should be capable of interrupting the maximum output current of the converter. One possibility is the standard series resonant (Schwarz) converter, which performs very well under short circuit conditions [2,12]. These converters could be used both to increase the source voltage for the distribution network and then to decrease it at the loads. Forced-commutated designs also should be considered, however, since they provide constant frequency operation as opposed to the variable frequency of most resonant converters. This feature reduces the size of the power transformer and may lower the EMI frequency range.

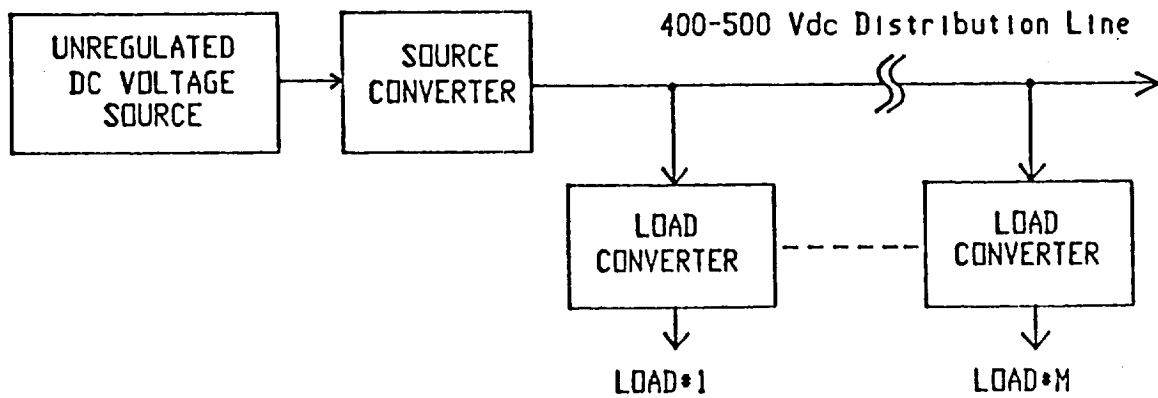


Fig. 2.1 High voltage dc distribution system

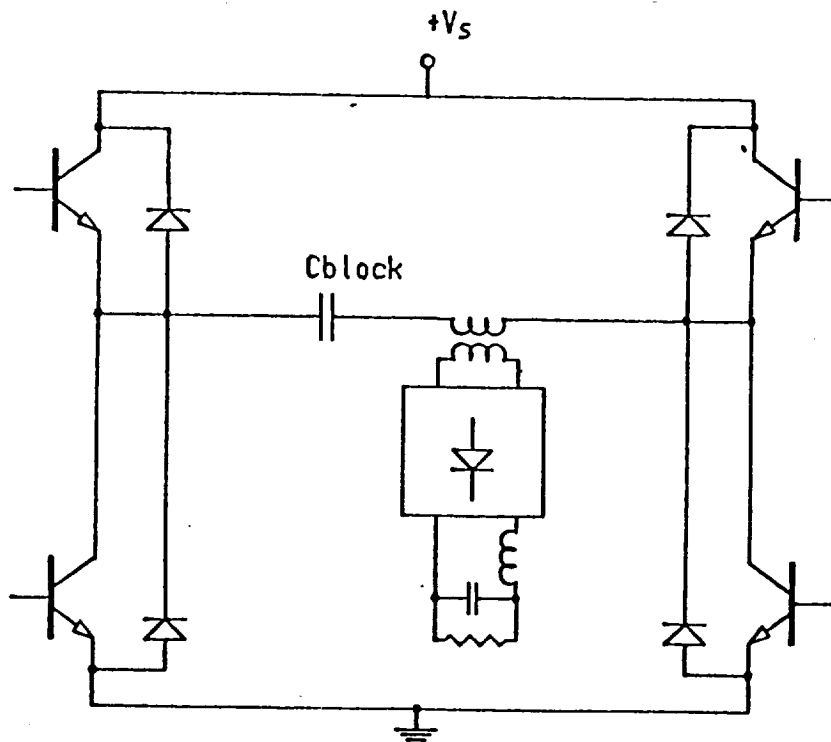


Fig. 2.2 PWM converter with blocking capacitor.

Since many of these converters must use a transformer at fairly high power levels, it seems best to concentrate on topologies that are immune from the current transients that can occur due to transformer flux imbalance. Some possibilities are listed below:

1. PWM bridge converter with a series blocking capacitor. One example of this is the PWM converter in Fig. 2.2. One obvious disadvantage to this approach is the rather large size of this capacitor at high power levels.
2. Schwarz or series resonant converter in Fig. 2.3. This circuit has been used in numerous high power applications, but it does require variable frequency operation to achieve natural commutation. This increases the size of the output transformer and widens the EMI frequency range. This circuit can be operated in a PWM mode at fixed frequency, but this also means forced commutation. It is questionable whether this forced mode has any true advantage over other PWM methods such as current mode control.
3. Push-pull current fed converters such as that in Fig. 2.4. This circuit was studied extensively in [14], and it enjoys the advantages of buck-boost operation and relatively simple control. The switching losses are relatively high however, especially because of the energy stored in the leakage inductances. Transistor voltages will also be quite high, making this circuit difficult to implement for high input voltages.
4. Current mode control (CMC) converter in Fig. 2.5. If properly designed, this converter would probably have a smaller volume than any of the others. Experience indicates that its controller is very sensitive to EMI problems however, and the technical literature contains very little information about high power applications of CMC.

### **High Frequency AC**

Fig. 2.6 shows a simplified block diagram for a 20 kHz distribution system. At least three different methods of generating the 20 kHz waveform have been proposed [2,6,18], but

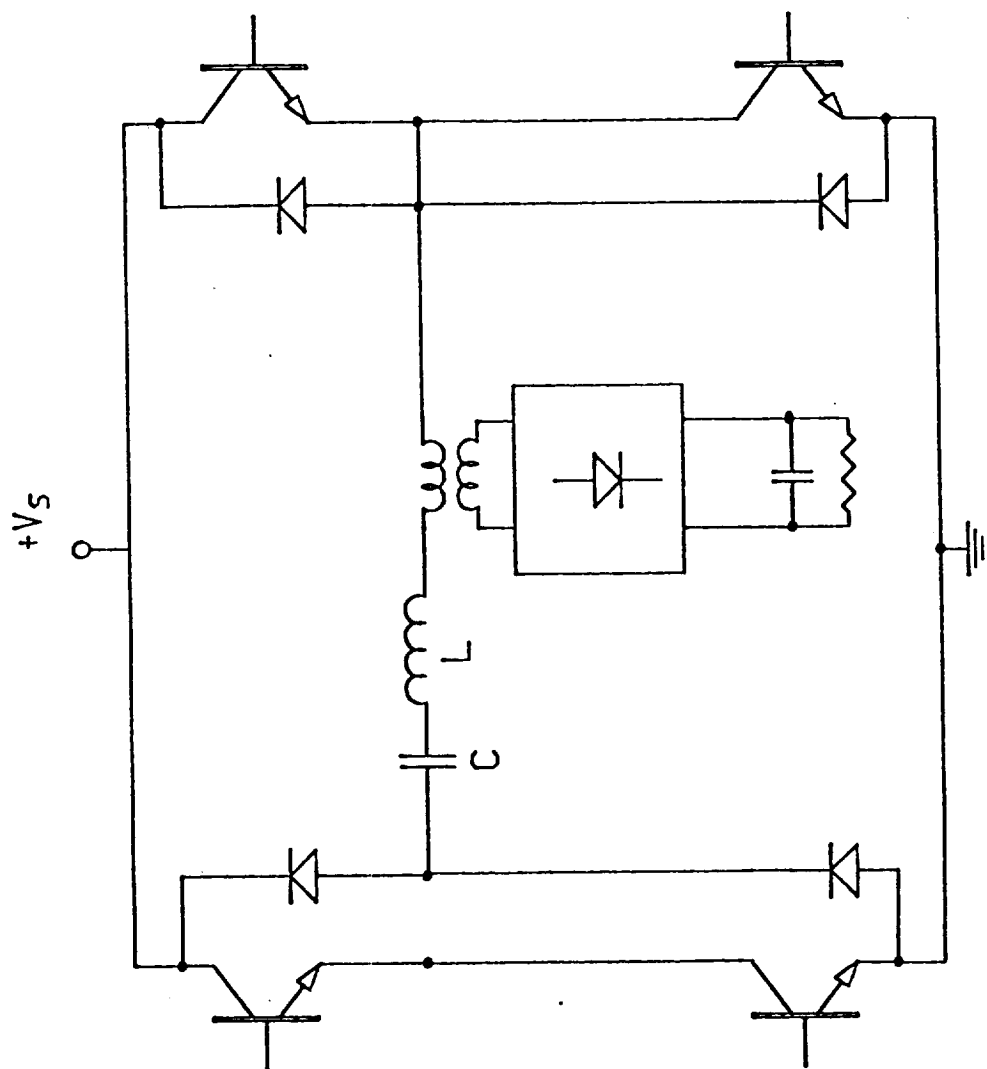


Fig. 2.3 Schwarz converter.

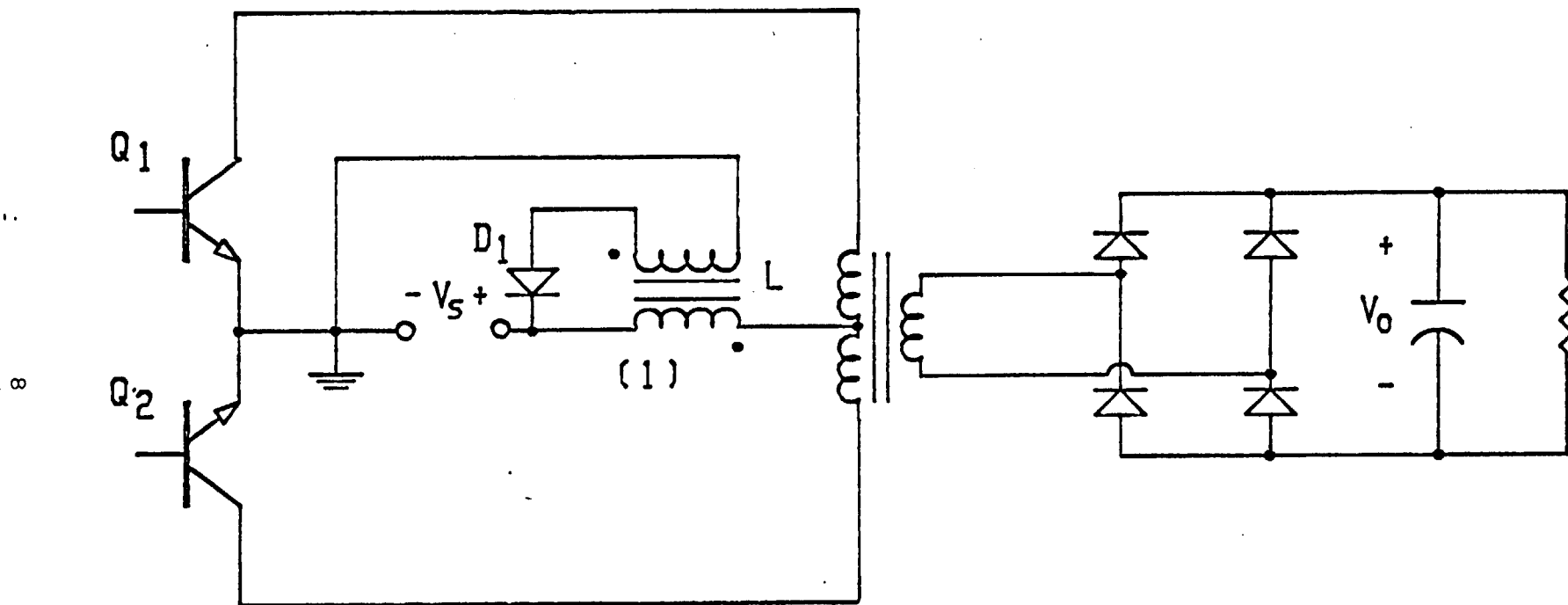
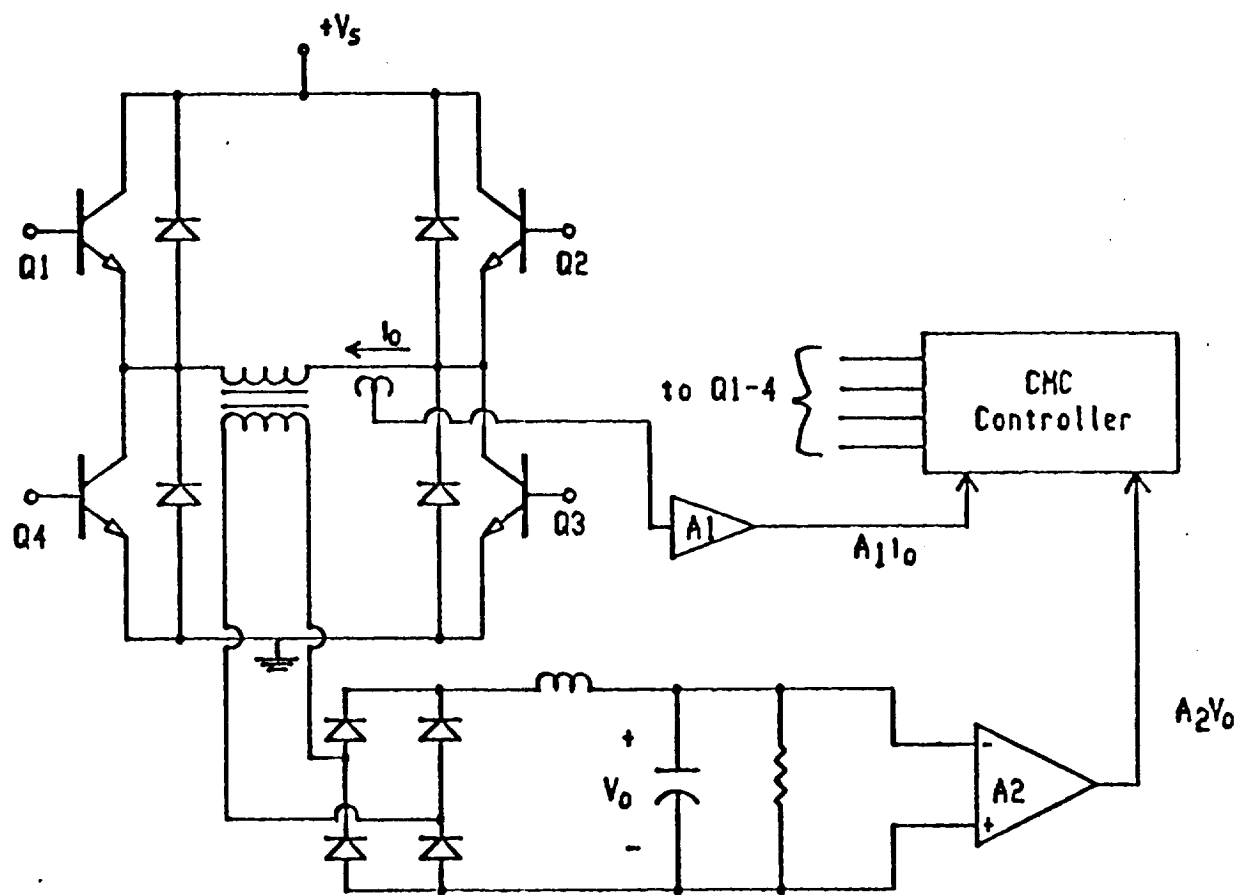


Fig. 2.4 Push-pull current-fed converter.



$A_1$  = Instantaneous current sensor

$A_2$  = average voltage sensor

Fig. 2.5 Full bridge converter with current mode control (CMC).

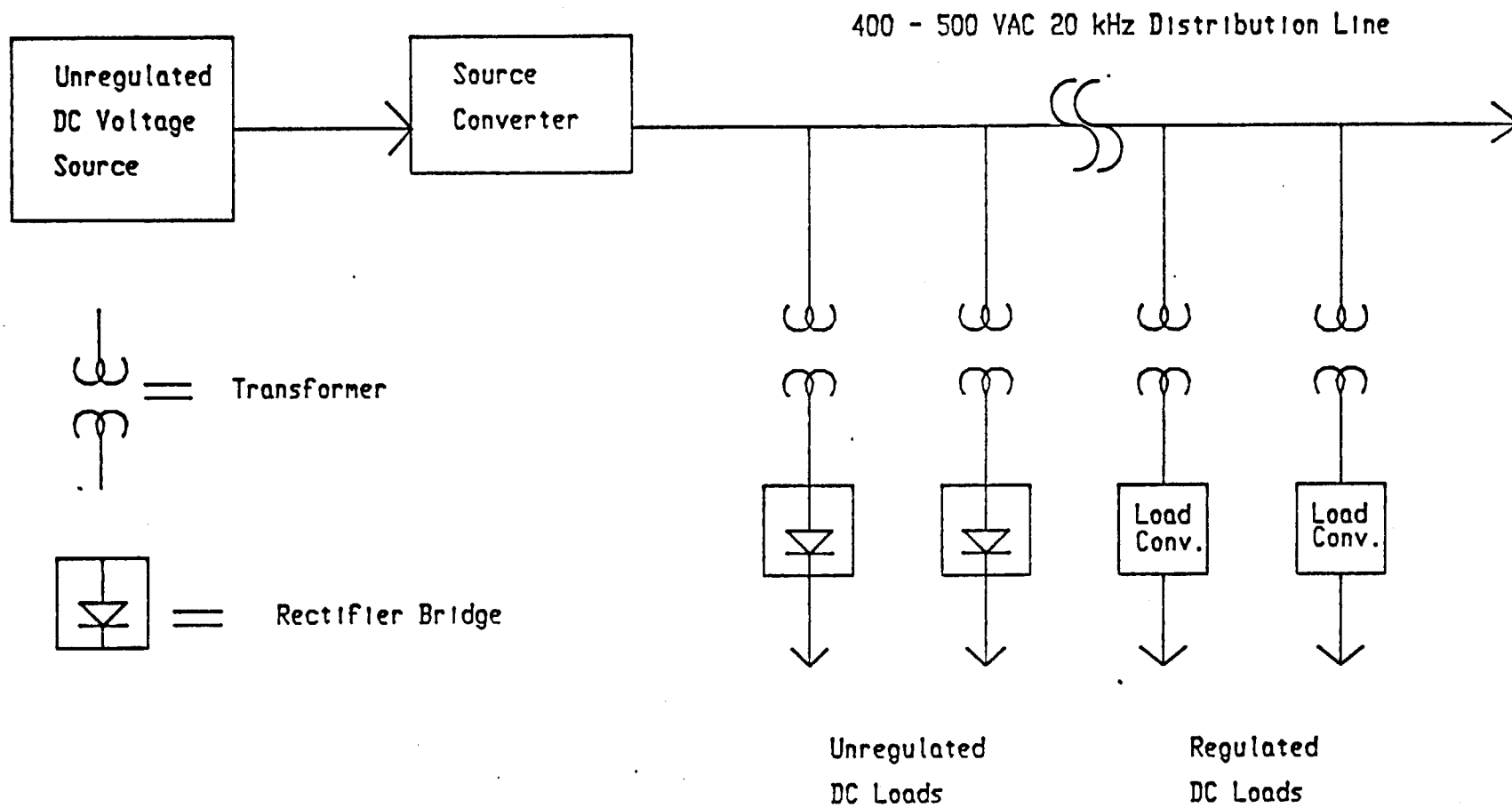


Fig. 2.6 AC distribution system.



all of these use a resonant circuit in the output stage. This is done to produce either a sinusoidal voltage or current at the output.

The main advantage of 20 kHz is the obvious one, namely simple voltage scaling with low-weight transformers. Two important consequences of this are the relatively simple converters that can be used for regulated loads, and the absence of converters for unregulated loads. However, EMI will probably be more of a problem than with dc because of the 20 kHz power on the distribution cables. Special low inductance, high capacitance cables must be used to reduce series voltage drop.

There are also indications that fault protection for a 20 kHz system will be more difficult than a dc system. While it is true that the zero current crossing of low frequency ac helps to extinguish the arc in an electro-mechanical breaker, the same cannot be said at 20 kHz. This is because the electric field strength recovery at 20 kHz is faster than the dielectric strength recovery, meaning that the current does not remain at a low value for a long enough time to allow the arc to extinguish [3]. This same reference also states that 20 kHz may require the use of more complex vacuum circuit breakers.

As with a dc system, the converters themselves must be fault tolerant, and they should be capable of withstanding a short circuit directly at their outputs. Again, this limits the necessary current ratings for the circuit breakers as well as protecting the converter. Blinking the source to allow the breakers to open at no load is still possible, but breaker ratings should not depend on this.

Only the source converters for generating the 20 kHz waveform will be considered here, since very standard converters can be used at the loads. Some possibilities are:

1. Phase-controlled, parallel-loaded resonant converter with the block diagram shown in Fig. 2.7. Of the various alternatives, this one has probably received the most attention, and a system of this type using two Mapham inverters (Fig. 2.8) has been proposed for driving 20 kHz distribution networks [6,7]. The two converters produce two sinusoidal output voltages that are added by the series transformer connection. Regulation is achieved by

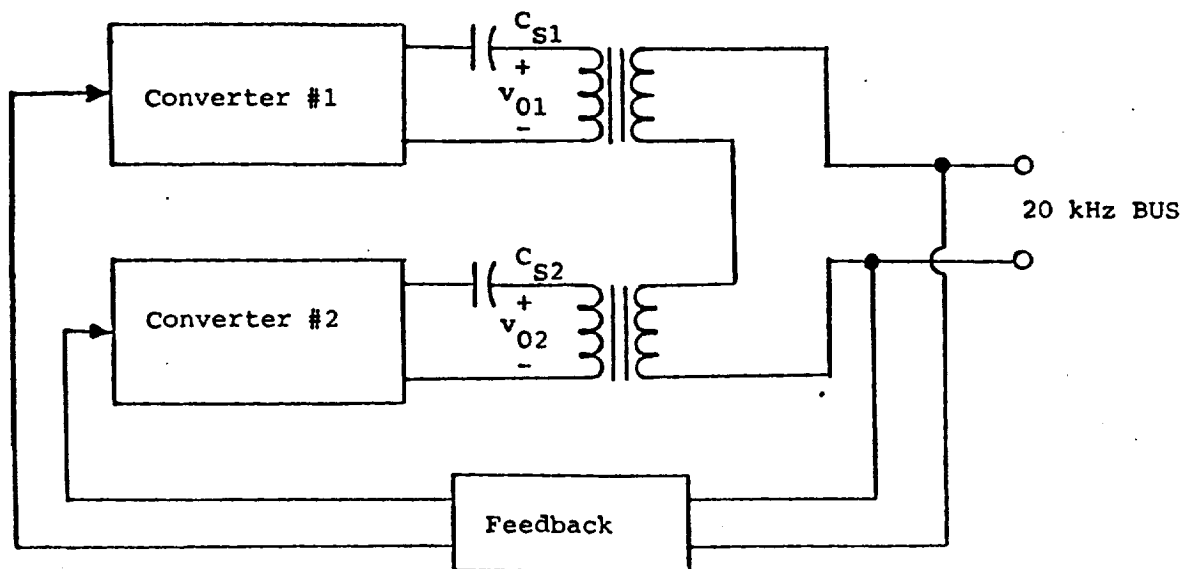


Fig. 2.7 Phase controlled parallel loaded converter system.

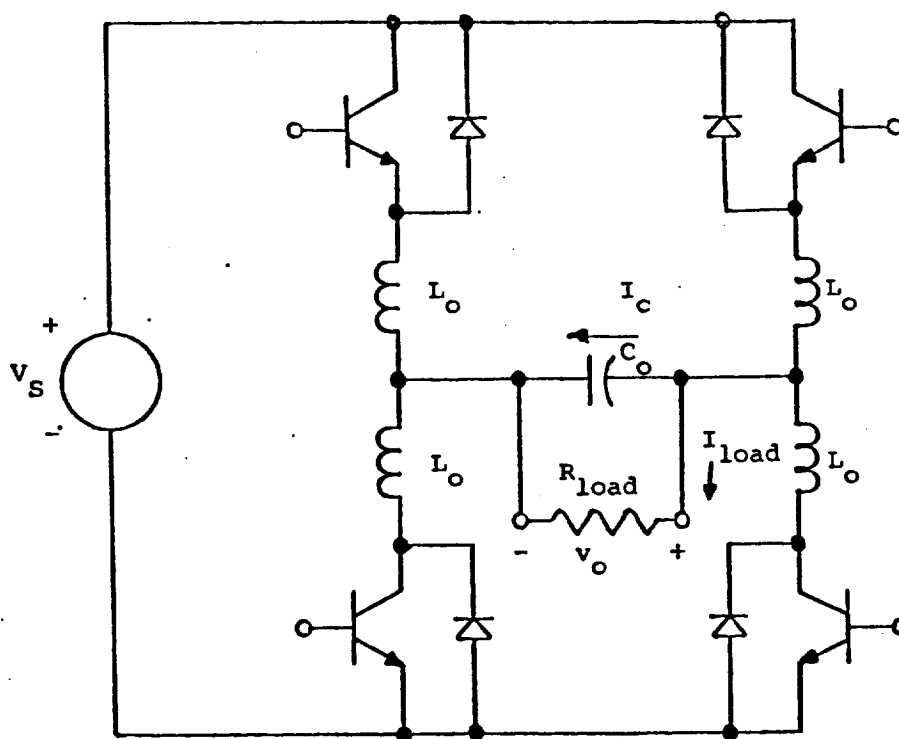


Fig. 2.8 Full bridge Mapham converter.

variation of the phase shift between the two, and  $C_{s1}$  and  $C_{s2}$  are added to help provide load regulation and short circuit protection. A similar implementation using two parallel-loaded half-bridge converters is given in [5]. Systems of this type can produce a low-distortion sinusoidal output voltage, but this is achieved by maintaining a current in  $C_o$  that may be as much as four times greater than the full load current. Mapham's original paper [4] illustrates this point with a design example for a 1KW half bridge circuit:

$$V_o = 118 \text{ V rms}, I_{load} = 8.5 \text{ A rms}, C_o = 4.7 \mu\text{F}.$$

operating frequency  $f_o = 10 \text{ kHz}$ , resonant frequency  $f_r = 13.5 \text{ KHz}$ . This indicates a capacitor current,  $I_c$ , of

$$I_c = 118 (2 \pi f_o C_o) = 34.85 \text{ A rms}.$$

therefore,  $I_c = (4.1) I_{load}$ .

As pointed out in [5], systems similar to Fig. 2.7 suffer another disadvantage in that the maximum current of one of the two converters occurs at an intermediate load instead of full load. Reference [5] includes data for a half-bridge, phase-controlled, parallel-loaded converter that indicates that the maximum transistor current in one of the two converters does not occur at full load. The maximum value for this current is actually about 1.75 times the full load value, which indicates that the current ratings for the transistors in one converter must be even higher than those indicated by the previous example. In regard to short circuit protection, experience with a similar circuit [14] indicates that achievement of this characteristic may require the use of forced commutation during the fault.

2. Cascaded Schwarz or series-loaded resonant converter/inverter with the schematic shown in Fig. 2.9 [1,2,8,9,11-14] and waveforms in Fig. 2.10. The development of this circuit is partially motivated by the special requirements for power systems supplied by nuclear reactors. The block diagram of a typical system is shown in Fig. 2.11. As noted earlier, these systems are expected to operate at power levels in excess of 100 kW and at rather low dc source voltages, e.g., 100 Vdc. This particular system uses a thermoelectric converter to transform heat from the nuclear reactor to electric energy. To reduce the amount of radiation

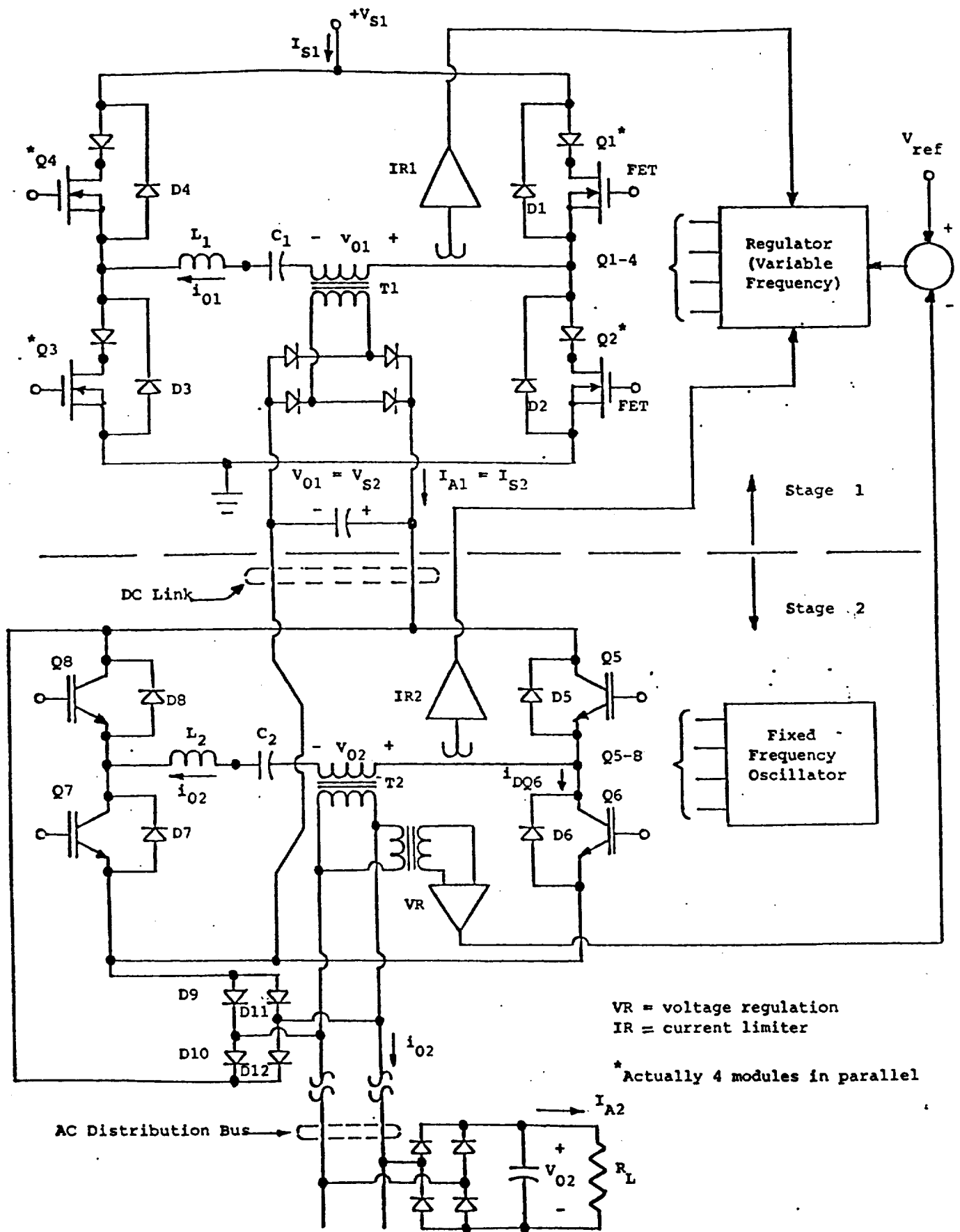
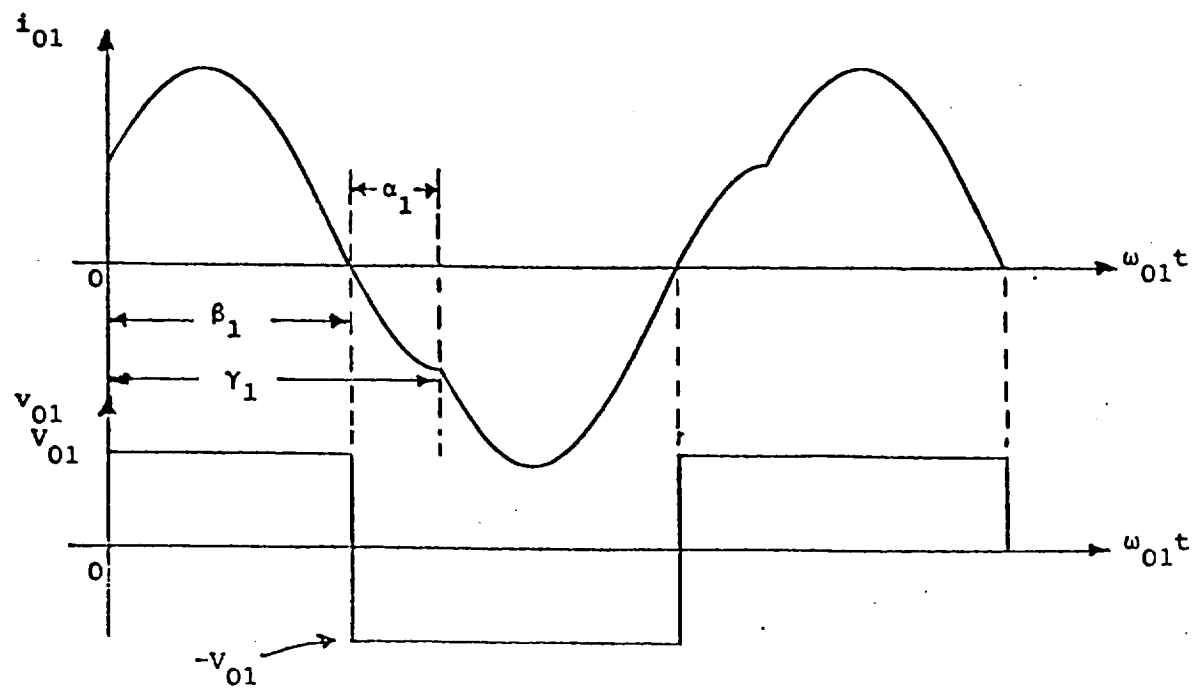
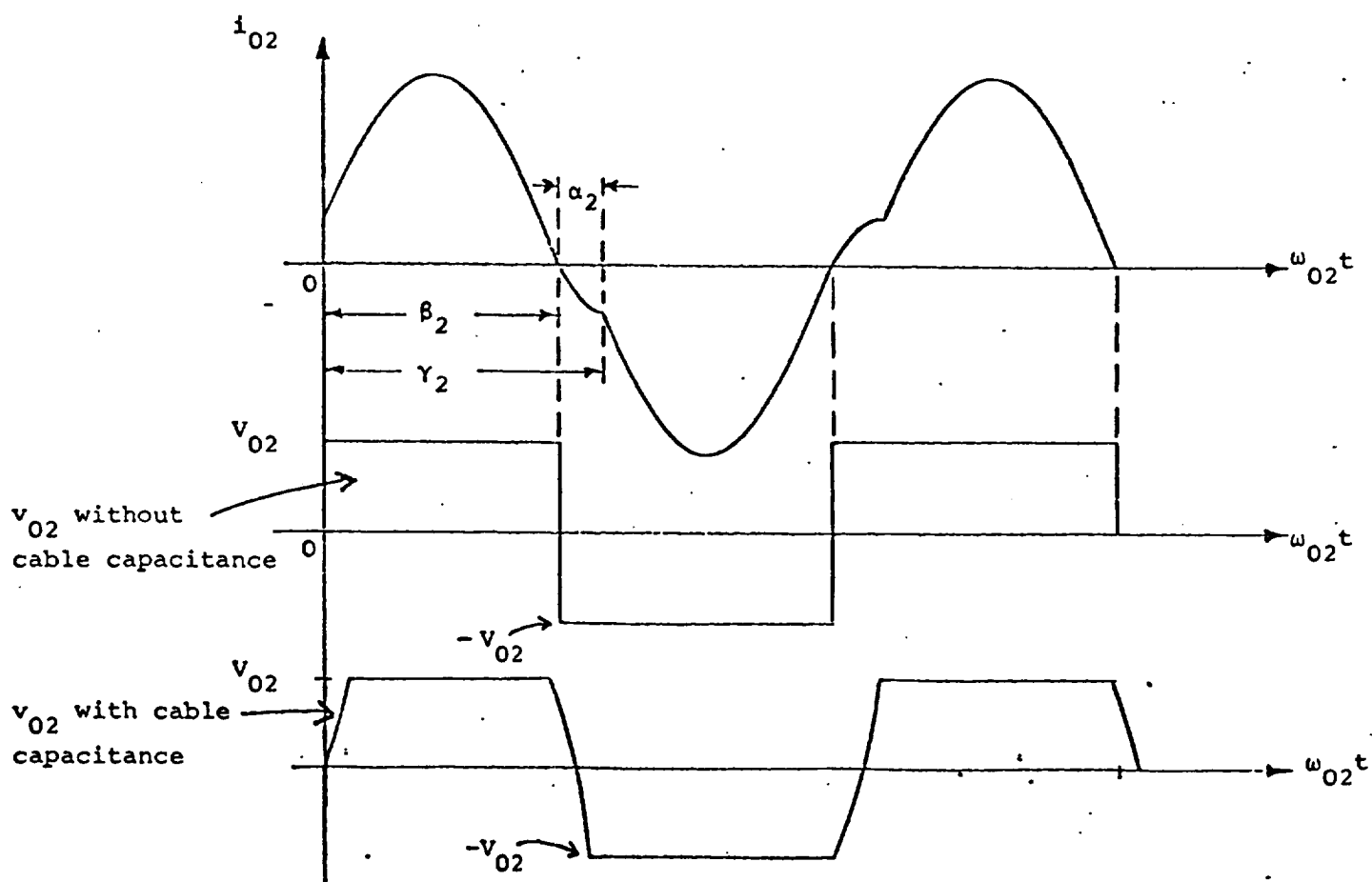


Fig. 2.9 Cascaded Schwarz converter.



(a) First Stage (variable frequency)



(b) Second Stage (fixed frequency)

Fig. 2.10 Typical output waveforms.

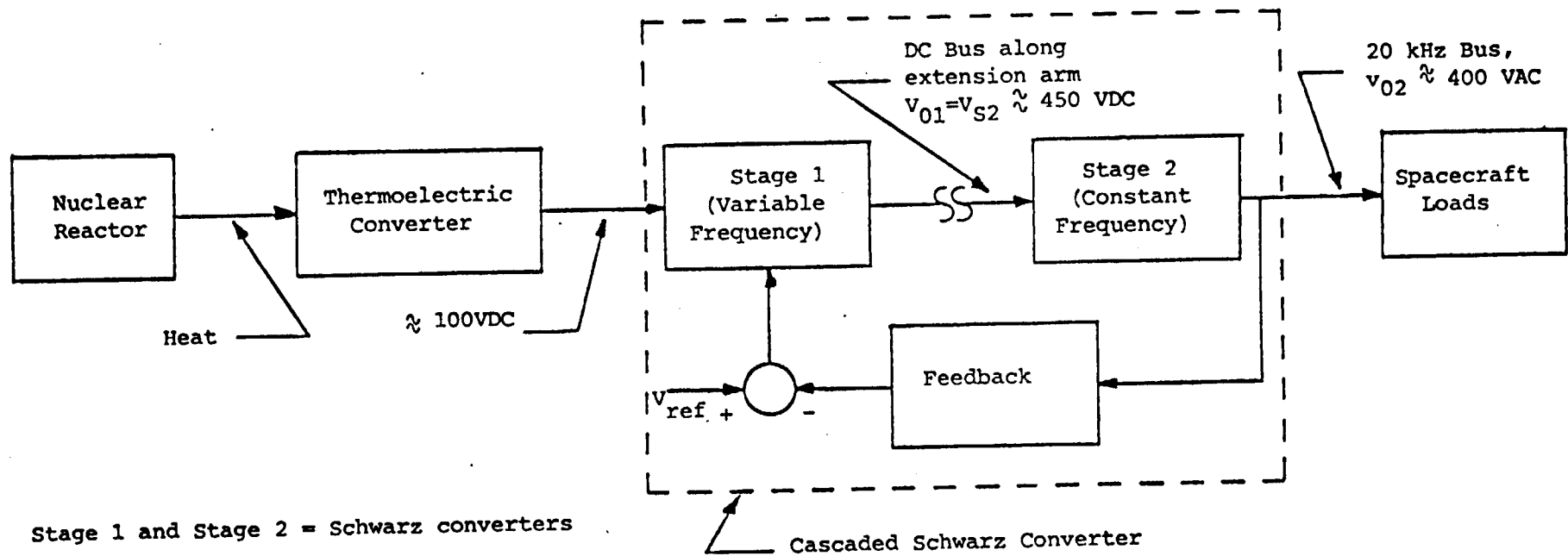


Fig. 2.11 20 kHz power system using cascaded Schwarz converter.

shielding and thus weight, the nuclear reactor and thermoelectric converter will be located on an extension arm away from the spacecraft. Since the typical source current may exceed 1000 A dc, it is also advisable to place an electronic converter near the reactor to increase the voltage and thus decrease cable weight.

For the example system in Fig. 2.11, power is transported down the extension arm at about 450 V dc using a relatively simple dc transmission cable. AC distribution is derived from a second converter operating at a fixed frequency of 20 kHz and located at the spacecraft. Regulation of the 20 kHz bus voltage,  $V_{02}$ , is achieved by variation of the DC bus voltage,  $V_{01} = V_{s2}$ .

The main advantages of this circuit are its relative simplicity and the inherent fault tolerance of each stage. Actually, the system does not require a Schwarz converter for the first stage, and any fault tolerant, controllable voltage source will suffice. One alternative converter that uses PWM to avoid the temperature limitations of the polypropylene resonant capacitor is analyzed in [14]. A three phase version is also possible, and a system of this type was studied in [8,9]. Three phase systems should reduce filtering requirements for rectified loads, but they do not appear to produce any significant savings in conductor weight. They also do not provide any special advantages for ac motors since these machines require power at a lower frequency.

This system produces a square wave output voltage which becomes trapezoidal as the cable capacitance increases. As shown in [2,12], the current tends to be sinusoidal, even with a rectified load. The other proposed systems produce a sinusoidal voltage, but with rectified loads, their current waveforms will approach a square wave.

This seems to be an important difference until it is noted that none of the anticipated loads appears to be sensitive to waveshape. Heating and lighting can use the 20 kHz directly, regardless of waveform, and all dc power supplies will be rectified and filtered. AC motors cannot use 20 kHz directly, so they too are insensitive to its waveshape. Thus it makes little difference whether the waveform is a sine wave, a square wave, or a trapezoid.

3. DC-inductor resonant inverter shown in Fig. 2.12. This system has been proposed for spacecraft power systems by TRW, Inc. [15,18]. It features a sinusoidal output voltage, appears to be relatively simple, and the above references indicate that its output is short circuit tolerant. Transistors Q3 and Q4 must be force commutated (PWM), whereas the two previous systems use natural commutation throughout. However, with the faster switching devices now becoming available, forced commutation may not be a significant drawback at 20 kHz, and an efficiency of 90% above 6 kW has been reported [18].

The circuit operates in the following manner. During the first half cycle, Q1 and Q3 are switched on with Q2 and Q4 off, and energy is supplied to the LC tank. Regulation is achieved by turning Q3 off at the appropriate time (PWM), causing D1 to conduct. Q1 remains on for the entire half cycle to allow the completion of this first half of the sinusoidal output voltage. The next half cycle is the same with Q2 and Q4 on while Q1 and Q3 are off.

One area of concern is an instability at light loads which was reported in [18]. This problem may have since been corrected, but the stability issue should be clarified and properly analyzed.

### **Summary**

In making the choice between a dc and an ac system, there are certain basic considerations which provide some guidance. As the power level increases, the voltage must also increase to restrain cable weight. However, as the voltage increases it ultimately reaches a level that is inconvenient to the user. This means the voltage must be scaled back down at the loads to reach a level that is compatible with the switching devices in the load converters. AC now has an important advantage because of its simple scaling with transformers.

However, ac also introduces such complications as more complex source converters, special cables, higher EMI, and probably more complex circuit breakers. This implies that dc is advantageous until the voltage gets so high that it becomes difficult to find converter components.



20kHz AC

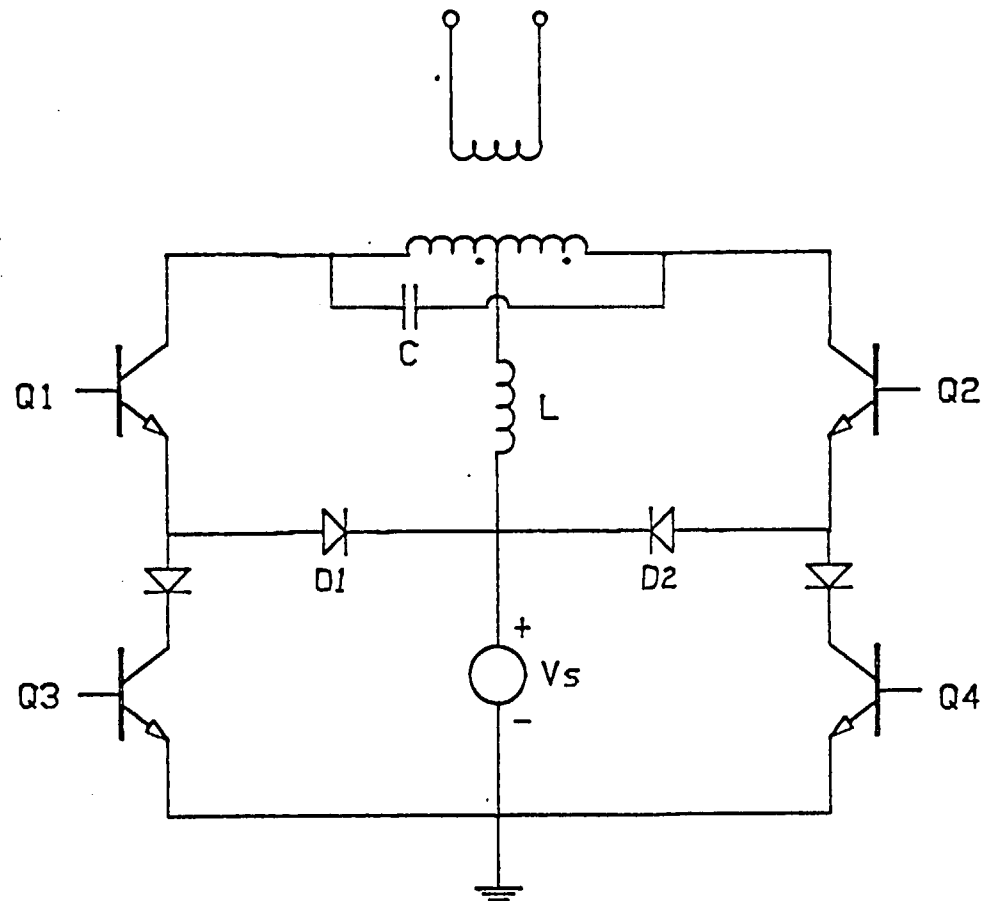


Fig. 2.12 DC inductor resonant inverter (TRW).

The remaining question is: At what voltage does this transition occur? Since the level is constantly increasing, it is difficult to place a maximum value on this voltage, but 1000 volt, 35 amp (@  $T_c = 90^{\circ} \text{ C}$ ) IGTs are presently available [19]. This indicates that high power converters switching at 20 kHz and using input voltages of 500 Vdc are within the range of present technology. It also seems quite likely that this level will increase as new devices such as the MCT become available.

### III. ANALYSIS OF NON-RESONANT TOPOLOGIES

#### INTRODUCTION

The analyses of the non-resonant dc-dc converter topologies will be undertaken to produce the information needed to compare the alternatives in the following areas:

- 1 ) Device utilization (voltage and current ratings relative to power processed).
- 2 ) Conduction losses.
- 3 ) Switching losses.
- 4 ) Ratings of transformers and reactive components.

It is expected that this comparison will aid in selecting the best topology for a given application.

The switch ratings and conduction losses will be calculated based on idealized operation. There are two categories of devices to be considered here: Ohmic devices, for which the voltage drop is modeled as being proportional to current, and constant-voltage-drop devices, for which the voltage drop is modeled as being independent of current. The first category includes MOSFETs, for which the following on-resistance ( $R_{DS}$ ) model will be used:

$$R_{DS} = K V_{DS}^{2.5}, \quad (3.1)$$

where  $K$  is proportional to the die area and  $V_{DS}$  is the rated drain-source breakdown voltage.

The constant-voltage-drop model will be used for diodes, BJTs, IGTs, and thyristors. The device voltage drop is approximated by its average value, perhaps 1 volt for diodes and BJTs, or 2 volts for thyristors.

Switching losses are somewhat elusive to quantify for several reasons. First, they are very dependent on the type of switch being used and its drive circuitry. Switching losses are also quite dependent on the size and type of snubber used. Generally it is found that increasing snubber size results in decreasing switching losses, but increasing snubber losses. There is an optimum-sized snubber which results in minimum overall losses [20]. However, the

optimum switching and snubber losses still remain a function of the voltage and current levels at the switch. The various topologies will therefore be compared in terms of the peak current interrupted (and the clamping voltage), and the peak blocking voltage at turn-on (and the current initially picked-up).

Transformer size and weight is a function of the maximum applied volt-second-integral (VSI) and the rms winding current(s). It is assumed here that the same core material and peak flux density is to be used in each switching converter under consideration. Transformers can be usefully rated in terms of rms volts and rms amperes if sinusoidal voltage is assumed. Because the voltages appearing in the dc-dc converters are generally not sinusoidal, and may not be comparable in all cases, transformer size will be compared on the basis of the VSI and winding currents.

The sizes and weights of reactive components are related to the peak stored energy. This will be used as a basis of comparison, therefore. The reactive components will generally be assumed large enough to ensure low-ripple operation in the analysis to follow. This greatly simplifies the analysis. Although this assumption is questionable in terms of low-power design practice, at high-power it is quite realistic in light of the necessity of presenting low-ripple dc voltages and currents at the ports of the converter.

## **BUCK CONVERTER**

The buck converter in its various forms which include a transformer is probably the most widely-used topology at the 1-10 kW level. Three basic possibilities are illustrated in Fig. 3.1. These three variations--the full-bridge, the half-bridge and push-pull topologies--are presented with component values resulting in equivalent performance at the input and output terminals. The full-bridge converter of Fig. 3.1 (a) is analyzed first and used as the reference for comparison with the others.

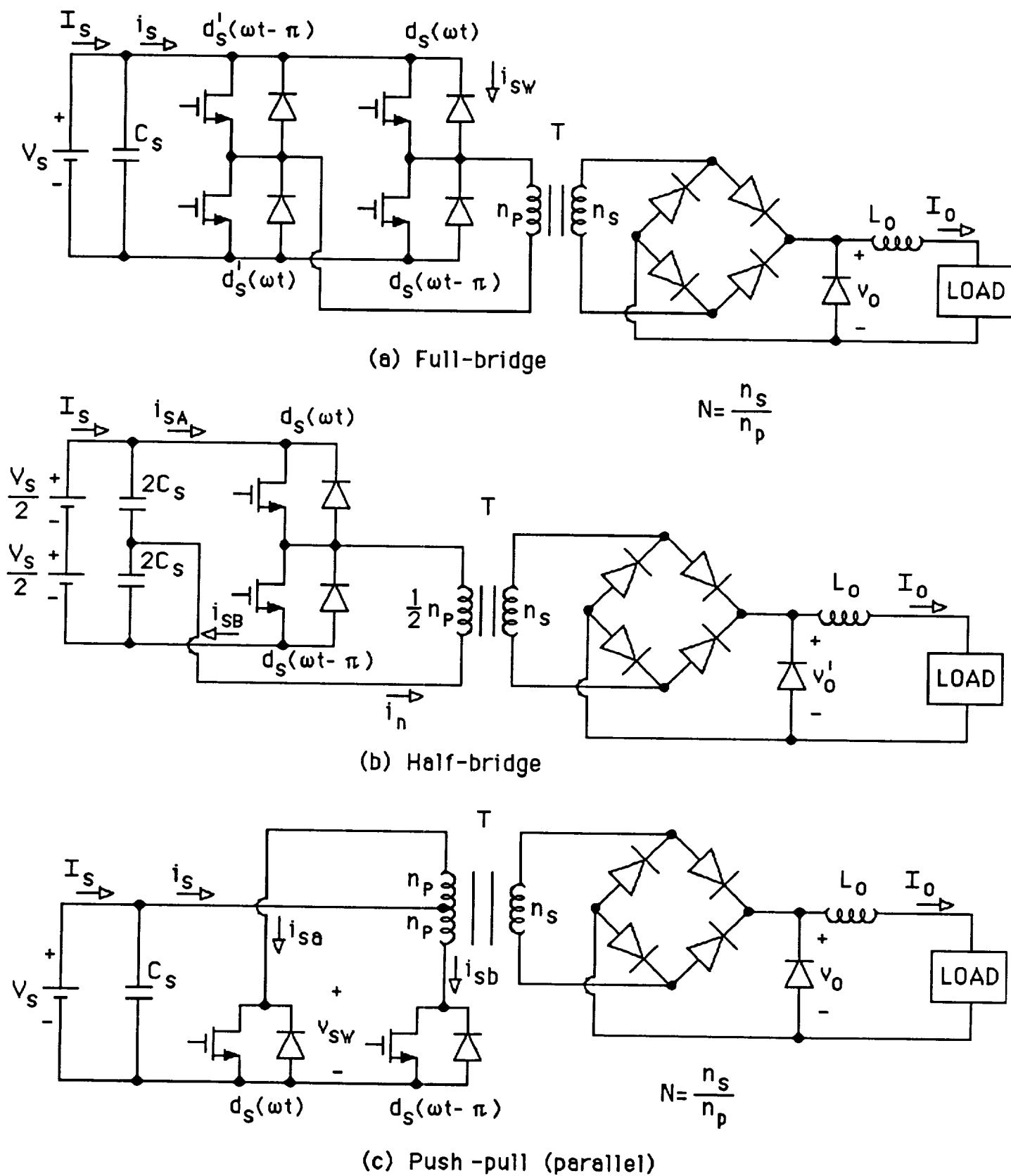


Fig. 3.1 Three versions of the buck converter using a transformer.

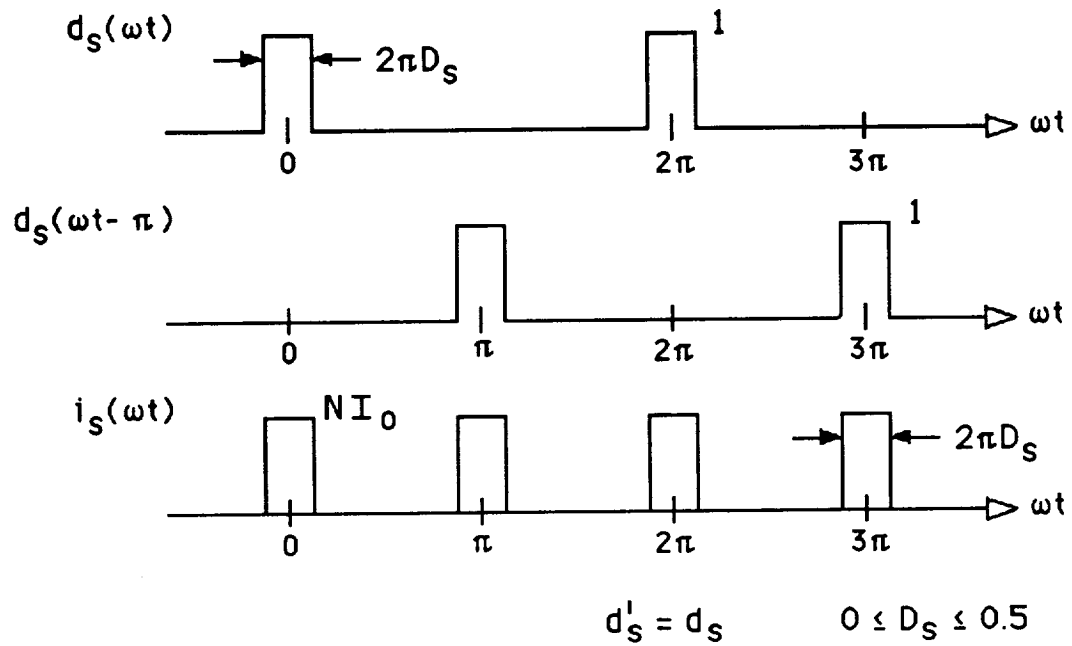


Fig. 3.2 PWM-switch gating waveforms.

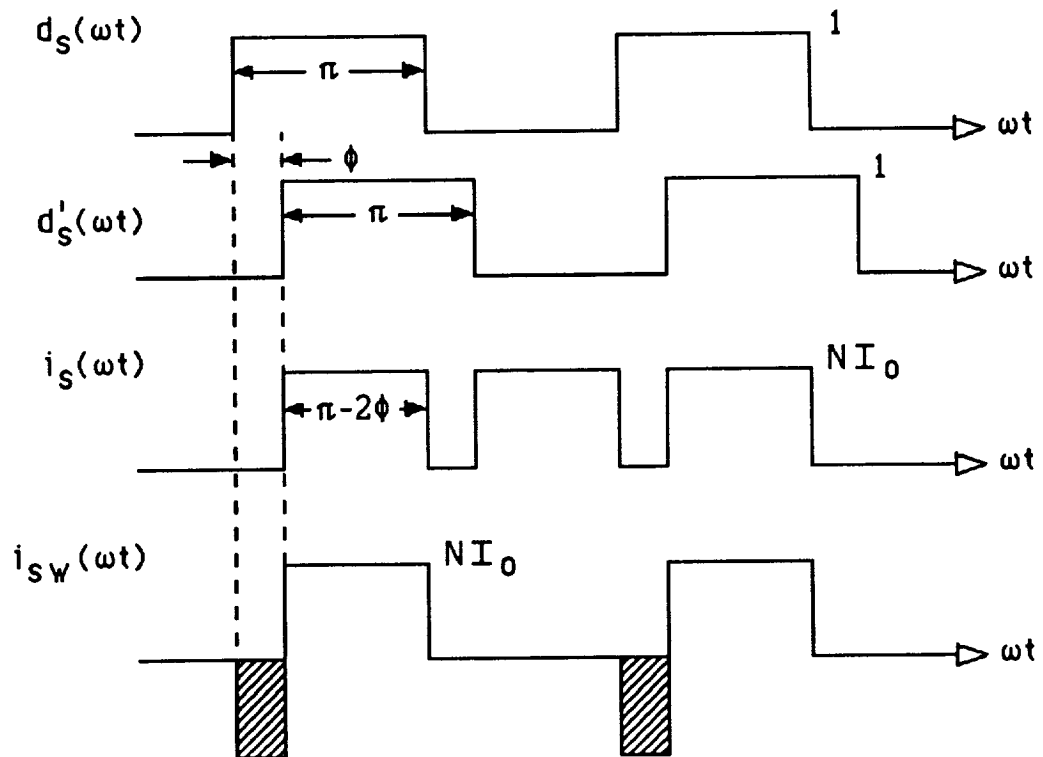


Fig. 3.3 Phase-shift-gating waveforms.

### Full-Bridge Buck Converter

Two different gating waveforms are illustrated in Figs. 3.2 and 3.3. The first, referred to as PWM, is the standard approach. The second, referred to as phase-shift gating, has been suggested as a means of reducing switching losses [21], although it produces results similar to those of PWM. The analysis of Fig. 3.1(a) begins with the Fourier-series representation of  $d_s(\omega t)$ :

$$d_s(\omega t) = D_s + \frac{2}{\pi} \sum_{n=1}^{\infty} \frac{1}{n} \sin(n\pi D_s) \cos n\omega t \quad (3.2)$$

With PWM the input current  $i_s$  can be written:

$$i_s(\omega t) = d_s(\omega t) NI_o + d'_s(\omega t - \pi) NI_o \quad (3.3)$$

As illustrated in Fig. 3.2,  $d'_s = d_s$  in the PWM approach. Note that  $NI_o$  is the output-side current reflected to the transformer primary. Therefore:

$$\begin{aligned} i_s(\omega t) &= 2D_s NI_o + \frac{2NI_o}{\pi} \sum_{n=1}^{\infty} \frac{1}{n} \sin(n\pi D_s) \cos(n\omega t) \\ &+ \frac{2NI_o}{\pi} \sum_{n=1}^{\infty} \frac{1}{n} \sin(n\pi D_s) \cos(n\pi) \cos(n\omega t). \end{aligned} \quad (3.4)$$

The above reduces to:

$$i_s(\omega t) = 2D_s NI_o + \frac{4NI_o}{\pi} \sum_{n=2}^{\infty} \frac{1}{n} \sin(n\pi D_s) \cos(n\omega t) \quad (3.5)$$

for  $n$  even.

Based on (3.5), the dominant ( $n=2$ ) harmonic current supported by the bypass capacitor has an amplitude of:

$$|i_{s2}| = \frac{2NI_o}{\pi} \sin(2\pi D_s) \text{ (A peak)}. \quad (3.6)$$

The dc input current is found from (3.5):

$$I_s = 2D_s NI_o \quad (3.7)$$

It can be seen that the effective duty cycle is  $2D_s$ , twice that of any individual switch.

The rms value of the input current  $i_s$  can be found by reference to Fig. 3.2:

$$i_s(\text{rms}) = NI_o \sqrt{2D_s} = \frac{I_s}{\sqrt{2D_s}} \quad (3.8)$$

The rms bypass-capacitor current is therefore:

$$\begin{aligned} i_{sc}(\text{rms}) &= \sqrt{\left(\frac{I_s}{\sqrt{2D_s}}\right)^2 - I_s^2} = I_s \sqrt{\frac{1-2D_s}{2D_s}} \\ &= NI_o \sqrt{2D_s(1-2D_s)} \end{aligned} \quad (3.9)$$

In terms of a given load current  $I_o$ , the rms capacitor current maximizes for  $D_s=0.25$  and is equal to:

$$i_{sc}(\text{rms} - \text{max}) = \frac{NI_o}{2} \quad \text{for } 2D_s = 0.5. \quad (3.10)$$

The amplitude of the ripple voltage appearing across  $C_s$  due to its finite value is estimated assuming that all of the ripple current flows through it, and considering only the dominant second harmonic.

$$|v_{s2}| \cong \frac{|i_{s2}|}{2\omega C_s} = \frac{NI_o \sin(2\pi D_s)}{\pi\omega C_s} \quad \text{V peak} \quad (3.11)$$

A more accurate estimate of the peak ripple voltage is found by integrating the ripple current passing through  $C_s$ :

$$\begin{aligned} |V_{SR}| &= \frac{1}{2} V_s (\text{p-p}) = \frac{1}{2C_s} \int_0^{D_s T} (NI_o - 2D_s NI_o) dt \\ &= \frac{NI_o}{4C_s f} (2D_s)(1-2D_s) (\text{V peak}). \end{aligned} \quad (3.12)$$

The transformer design is based primarily on the volt-second integral (VSI) and the rms winding currents. The required VSI is given by:

$$VSI = \frac{D_s V_s T}{n_p} = \frac{V_o T}{2n_s} \quad (3.13)$$

The rms current in the transformer primary is given by:

$$i_{PRI}(\text{rms}) = \sqrt{2D_s} NI_o = \frac{I_s}{\sqrt{2D_s}} \quad (3.14)$$



The secondary current is scaled according to the turns-ratio.

The output-side voltage  $V_o(\omega t)$  has the following series representation:

$$v_o(\omega t) = 2D_s NV_s + \frac{4NV_s}{\pi} \sum_{n=2}^{\infty} \frac{1}{n} \sin(n\pi D_s) \cos(n\omega t) \quad (3.15)$$

for  $n$  even.

From this series, the amplitude of the dominant second harmonic is seen to be:

$$|v_{02}| = \frac{2NV_s}{\pi} \sin(2\pi D_s) \quad \text{V peak.} \quad (3.16)$$

The amplitude of the ripple current in  $L_o$  is estimated based on (3.16) and the assumption that the ripple voltage is entirely supported by  $L_o$ :

$$|i_{02}| \equiv \frac{|v_{02}|}{2\omega L_o} = \frac{NV_s \sin(2\pi D_s)}{\pi \omega L_o} \quad \text{A peak.} \quad (3.17)$$

The amplitude of the ripple current can also be estimated by integrating the ripple voltage, assuming that all of it is supported by  $L_o$ :

$$\begin{aligned} |i_{OR}| &= \frac{1}{2L_o} \int_0^{D_s T} (NV_s - 2D_s NV_s) dt \\ &= \frac{NV_s}{4L_o f} (2D_s)(1-2D_s) \end{aligned} \quad (3.18)$$

Ripple factors  $R_V$  and  $R_I$  are defined to be the amplitudes of ripple voltage or current normalized with respect to the dc voltage or current. Using (3.12):

$$R_v = \frac{|v_{SR}|}{V_s} = \frac{N^2 I_o}{4C_s f V_o} (2D_s)^2 (1-2D_s) \quad (3.19)$$

Assuming that the design procedure sets the transformer turns ratio  $N = \frac{V_o}{V_s(\min)}$

$$R_v = \frac{V_o I_o}{\omega} \frac{2\pi}{4C_s V_s^2(\min)} (2D_s)^2 (1-2D_s)$$

which maximizes for the worst case

$$R_v(WC) = \frac{P_{DES}}{\omega} \frac{2\pi}{27C_s V_s^2(\min)} \quad (3.20)$$

when  $2D_s = 2/3$ .

Using (3.18):

$$\begin{aligned} R_I &\equiv \frac{|i_{OR}|}{I_o} = \frac{NV_s}{4L_o f I_o} (2D_s)(1-2D_s) \\ &= \frac{P_{DES}}{\omega} \frac{\pi}{2L_o I_o^2} (1-2D_s) \end{aligned} \quad (3.21)$$

Line regulation is assumed to be required so that it is useful to define "turn-down ratio"  $K_{TD}$ :

$$K_{TD} \equiv \frac{V_s(\max)}{V_s(\min)} \quad (3.22)$$

If the load voltage is regulated with  $2D_s = 1$  at  $V_s(\min)$ , then:

$$2D_s(\min) = \frac{V_s(\min)}{V_s(\max)} = \frac{1}{K_{TD}} \quad (3.23)$$

Therefore, the worst case for (3.21) is

$$R_I(WC) = \frac{P_{DES}}{\omega} \frac{\pi}{2L_o I_o^2(\max)} \frac{K_{TD}-1}{K_{TD}} \quad (3.24)$$

Note that the worst case for  $C_s$  is found in terms of the minimum supply voltage  $V_s$  for which full power operation is to be obtained. For  $L_o$ , the design is determined at the full-load current  $I_o(\max)$ . For load currents less than this,  $R_I$  increases.

The maximum stored energy for a design based on (3.20) and (3.24) is calculated using:

$$\begin{aligned} E_{CS} &= \frac{1}{2} C_s V_s^2(\max) \cdot (1 + R_v)^2 \\ E_{Lo} &= \frac{1}{2} L_o I_o^2(\max) \cdot (1 + R_I)^2 \end{aligned} \quad \text{and} \quad (3.26)$$

Therefore,

$$E_{CS} = \frac{P_{DES}}{\omega} \frac{\pi}{27} K_{TD}^2 \frac{(1 + R_v)^2}{R_v} \quad (3.27)$$

and

$$E_{Lo} = \frac{P_{DES}}{\omega} \frac{\pi}{4} \frac{K_{TD} - 1}{K_{TD}} \frac{(1 + R_I)^2}{R_I} \quad (3.28)$$

The switch ratings are next reviewed. If a circuit layout with low parasitic inductance in the current-commutating paths can be obtained, the blocking voltage on the switches is well-defined at

$$V_{sw} = V_s. \quad (3.29)$$

The switch current ratings are

$$i_{sw}(\text{rms}) = N I_o \sqrt{D_s} = \frac{I_s}{2\sqrt{D_s}} \quad \text{and} \quad (3.30)$$

$$i_{sw}(\text{avg}) = N I_o D_s = \frac{I_s}{2} \quad (3.31)$$

Therefore, the expected conduction loss per switch, assuming ohmic switches, is:

$$P_{OHM} = (N I_o)^2 D_s R_{DS} = I_s^2 \frac{R_{DS}}{4 D_s} \quad (3.32)$$

The greatest loss occurs at low line, for which the design power  $P_{DES}$  is equal to  $I_s(\max) \cdot V_s(\min)$ .

For this worst case, (3.32) can be written:

$$\left. \frac{P_{OHM}}{P_{DES}} \right|_{wc} = \frac{1}{2} \frac{I_s(\max)}{V_s(\min)} R_{DS} \quad (3.33)$$

Using (3.1) produces the following worst-case result, given as the total conduction loss for four ohmic switches:

$$\left. \frac{P_{COND}}{P_{DES}} \right|_{wc} = 2 I_s(\max) K K_{TD} V_s^{1.5}(\max) \quad (3.34)$$

This suggests that the die area (or number of paralleled devices) for a constant normalized conduction loss is proportional to maximum input current, but more than proportional to voltage level. Also, (3.34) shows the penalty of supplying line regulation. For constant-voltage-drop switches, the worst-case normalized loss per switch occurs at low line. The total conduction loss for four constant-voltage-drop switches is:

$$\frac{P_{COND}}{P_{DES}} = 2K_{TD} \frac{V_{SW}}{V_s(\max)} . \quad (3.35)$$

Switching losses are a function of the current interrupted, and the voltage blocked. At turn-on, the blocking voltage and current  $di/dt$  determine the switching losses. In Fig. 2.1(a), the blocked voltage is  $V_s$  and the picked-up current is  $NI_o$  with infinite  $di/dt$  at turn-on if the transformer is ideal. Leakage inductance lowers the  $di/dt$ ; a small amount is probably beneficial. The energy trapped in the leakage inductance is returned to the source  $V_s$  through the anti-parallel diodes at turn-off. Turn-on before this energy is completely returned will result in picking up a circulating current less than  $NI_o$  with  $di/dt$  limited only by the primary-side layout inductance. A minimum off-time could be imposed to prevent this possibility. This off time should exceed

$$t_{off} \geq \frac{NI_o L_{ep}}{V_s} , \quad (3.36)$$

where  $L_{ep}$  is the primary-reflected leakage inductance. The transformer magnetizing current will also cause a circulating primary-side current when all switches are off.

This current is also likely to be picked-up with high  $di/dt$  at turn-on; however, its magnitude will normally be a small percentage of the design full-load current and it is not expected to cause much additional switching loss.

Turn-on while significant current is circulating on the primary side of the transformer causes an additional difficulty due to the reverse-recovery of the antiparallel diodes. During the recovery transient, the source  $V_s$  is essentially shorted and shoot-through current rises at a rate limited only by the layout inductance. The diodes are characterized by a stored charge

equal to the product of their forward current prior to commutation and their transit time. This charge is removed through the reverse current together with internal recombination. In the case of a rapid commutation (low layout inductance), charge removal is primarily due to the reverse-recovery current. Fast recovery diodes, even at the expense of greater forward drop, are helpful in reducing this loss.

The turn-off process requires interrupting a current of  $NI_o$ , plus the peak ripple current, with a clamping voltage of  $V_s$ . Any layout inductance present on the primary side traps energy which causes voltage overshoot on the off-going switch. Snubbing generally involves a small series inductance (including the layout inductance) which controls the turn-on losses and peak diode recovery current, together with shunt elements to prevent voltage overshoot at turn-off. These may be dissipative, or energy-recovering. It is generally found that snubbing elements lower the switching losses in the switches by shifting them to the snubbers. There is usually an optimum snubber which minimizes overall loss [20].

### **Phase-Shift Gating**

Phase-shift gating has been proposed [21] as a means of lowering switching losses in the full-bridge configuration. Typical waveforms are illustrated in Fig. 3.3, where it can be seen that each switching pole is driven with 50-percent duty cycle, but variable phase relative to each other. The resulting input current and output voltage waveforms are the same as those of standard PWM, thus most of the previous design equations continue to apply. However, the switch current illustrated in Fig. 3.3 (refer also to Fig. 3.1) shows the possibility of reduced switching losses. If an ideal transformer were assumed, the shaded sections of  $i_{sw}$  would not be present, and it can be seen that this switch is turning on without loss. (The gating signal  $d_s$  is present prior to current flow, which is initiated by turn-on of the diagonal switch.) The two switches on the right-hand side of the bridge are found to suffer no turn-on losses, their conduction being initiated by turn-on of left-hand side switches. In a similar manner, the left-hand side switches have no turn-off loss. Ideally, the designer can then optimize the snubbers for turn-on (left side), or for turn-off (right side).

The situation illustrated in Fig. 3.3 might not occur in practice, however. The presence of significant leakage inductance in the transformer would permit the circulation of a current less than  $NI_o$  in the upper switches of the bridge during the shaded portion of  $i_{sw}$  in Fig. 3.3. Only diode voltage drops act to oppose this current during this time. The turn-off of the upper left-hand switch would interrupt this circulating current, and would therefore not be without loss. The evaluation of the practicality of this gating approach is ongoing [22], but so far experimental data have not produced any efficiency improvement attributable to this technique. Phase-shift gating is clearly not applicable to the half-bridge and push-pull topologies.

### **Half-Bridge Buck Converter**

The half-bridge buck converter of Fig. 3.1 provides the same performance at its terminals as the full-bridge version, so that many of the previous analytical results apply here. The differences will be uncovered in the following analysis. The switch existence function

$d_s(\omega t)$  is given by (3.2). The input side currents are therefore:

$$i_{SA}(\omega t) = d_s(\omega t) 2NI_o = 2D_s NI_o + \frac{4NI_o}{\pi} \sum_{n=1}^{\infty} \frac{1}{n} \sin(n\pi D_s) \cos(n\omega t) \quad (3.37)$$

$$i_{SB}(\omega t - \pi) = d_s(\omega t) 2NI_o = 2D_s NI_o + \frac{4NI_o}{\pi} \sum_{n=1}^{\infty} \frac{1}{n} \sin(n\pi D_s) \cos(n\pi) \cos(n\omega t) \quad (3.38)$$

Note that  $N$  is the turns ratio of the equivalent full-bridge transformer: the half-bridge circuit requires a ratio of  $2N$ . The dominant harmonic current in each of the input capacitors ( $2C_s$ ) is the fundamental and has an amplitude of:

$$|i_{SA1}| = \frac{4NI_o}{\pi} \sin(\pi D_s) \text{ A peak} \quad (3.39)$$

the dc input current is  $2D_s NI_o$  as before. The effective duty cycle is again  $2D_s$ , twice that of the individual switch. The rms value of  $i_{SA}$  or  $i_{SB}$  is:

$$i_{SA}(\text{rms}) = 2NI_o \sqrt{D_s} = \frac{I_s}{\sqrt{D_s}} \quad (3.40)$$

The rms bypass-capacitor current is therefore

$$\begin{aligned} i_{SC}(\text{rms}) &= \sqrt{\frac{I_s^2}{D_s} - I_s^2} = I_s \sqrt{\frac{1-D_s}{D_s}} \\ &= 2NI_o \sqrt{D_s(1-D_s)} \end{aligned} \quad (3.41)$$

In terms of a given load current  $I_o$ , the rms capacitor current maximizes for  $D_s = 0.5$  and is equal to:

$$i_{SC}(\text{rms-max}) = NI_o \quad \text{for } 2D_s = 1.0 \quad (3.42)$$

The amplitude of the ripple voltage appearing across either of the two capacitors can be estimated by assuming that all of the ripple current passes through it. It can be seen that fundamental-frequency ripple appears on each bypass capacitor; however, all odd-harmonic components cancel when adding the net voltage across both capacitors. Therefore, the second-harmonic ripple voltage for both capacitors is estimated:

$$|v_{s2}| \cong 2 \frac{|i_{SA2}|}{2\omega(2C_s)} = \frac{NI_o \sin(2\pi D_s)}{\pi\omega C_s} \text{ V peak} \quad (3.43)$$

For the half-bridge to have the same input voltage ripple as the full-bridge, (3.43) shows that each of its bypass capacitors must have twice the capacitance of that of the full-bridge. The rms current rating of each of these is twice that of the full-bridge, although each is rated at one-half the dc voltage.

The ripple voltages appearing on each of the bypass capacitors can be found by integrating their respective ripple currents:

$$\begin{aligned} v_{SAR} &= \frac{1}{2C_S} \int_0^t (i_{SA} - I_s) dt + IC \text{ and} \\ v_{SBR} &= \frac{1}{2C_S} \int_0^t (i_{SB} - I_s) dt + IC . \end{aligned} \quad (3.44)$$

The ripple voltage appearing at the input terminals is found by adding these two expressions:

$$v_{SR} = v_{SAR} + v_{SBR} = \frac{1}{2C_S} \int_0^t (i_{SA} + i_{SB} - 2I_s) dt + IC . \quad (3.45)$$

The peak ripple is one-half the peak-to-peak ripple, and is given by:

$$v_{SR} (\text{peak}) = \frac{1}{2} \frac{1}{2C_S} \int_0^{DT} (2NI_o - 4D_S NI_o) dt \quad (3.46)$$

This is seen to be the same as (3.12) for the full-bridge; therefore, the capacitor sizing and ripple voltage calculations of (3.19 - 3.20) apply to the half-bridge also. The total stored energy in both capacitors, when chosen according to (3.20), is

$$\begin{aligned} E_{CS} &= 2 \left[ \frac{1}{2} (2C_S) \left( \frac{1}{2} V_s(\text{max}) \right)^2 (1 + R_v)^2 \right] \\ &= \frac{1}{2} C_S V_s^2(\text{max}) \cdot (1 + R_v)^2 \end{aligned} \quad (3.47)$$

Thus,  $E_{CS}$  is also given by (3.27).

The half-bridge converter behaves the same as the full-bridge on its secondary side, therefore all results pertaining to the secondary side of the full-bridge continue to apply.



The switch voltage ratings continue to be the same as those of the full-bridge circuit. The current ratings are doubled, however.

$$i_{sw}(rms) = 2NI_o\sqrt{D_s} = \frac{I_s}{\sqrt{D_s}} \text{ and} \quad (3.48)$$

$$i_{sw}(avg) = 2NI_oD_s = I_s. \quad (3.49)$$

Ohmic switches would therefore need to have one-half the resistance of those of the full-bridge converter to maintain the same total conduction loss. Constant-voltage switches would need to have doubled current ratings for the half-bridge circuit. The expected per-switch conduction loss for the half-bridge circuit would be:

$$P_{OHM} = 4(NI_o)^2 D_s R_{DS} = I_s^2 \frac{R_{DS}}{D_s} \quad (3.50)$$

if ohmic switches were used, and

$$P_{CV} = 2NI_oD_s V_{SW} = I_s V_{SW} \quad (3.51)$$

if constant-voltage switches were used. Half-bridge and full-bridge topologies have the same total conduction loss for a given number of devices, provided paralleling with perfect current sharing is possible.

Switching losses related to commutation voltage will be similar to those of the full-bridge. However, the doubled primary-side peak current will cause increased sensitivity to layout inductance and current-related switching losses will be higher. They will only occur at two switches instead of four, however. A minimum off-time which will permit recovery of the energy trapped in the transformer leakage inductance is given by

$$t_{OFF} \geq \frac{4NI_oL_{ep}}{V_s}, \quad (3.52)$$

where  $L_{ep}$  is the primary-reflected leakage inductance. Because there are half as many primary turns for the half-bridge topology as that of the full-bridge, it is reasonable to assume that one-fourth the  $L_{ep}$  could be achieved in the half-bridge transformer, thus permitting the same off-time as that of the full-bridge.

### Push-Pull Buck Converter

The push-pull buck converter of Fig. 3.1 provides the same performance at its terminals as the full-bridge version. the internal differences are uncovered in the following analysis. Based on the switch existence function (2.2), the switch currents are:

$$\begin{aligned} i_{sa} &= d_s(\omega t)NI_o \\ &= D_sNI_o + \frac{2NI_o}{\pi} \sum_{n=1}^{\infty} \frac{1}{n} \sin(n\pi D_s) \cos(n\omega t) \end{aligned} \quad (3.53)$$

and

$$\begin{aligned} i_{sb} &= d_s(\omega t - \pi)NI_o \\ &= D_sNI_o + \frac{2NI_o}{\pi} \sum_{n=1}^{\infty} \frac{1}{n} \sin(n\pi D_s) \cos(n\pi) \cos(n\omega t). \end{aligned} \quad (3.54)$$

The input current  $i_s$  is equal to the sum of  $i_{sa}$  and  $i_{sb}$ ; it is therefore the same as (3.4) and all conclusions related to  $C_S$  for the full-bridge topology apply here as well.

The effective duty cycle is  $2D_s$ ; the dc input current is

$$I_s = 2D_sNI_o. \quad (3.55)$$

The transformer volt-second integral (VSI) is the same as for the other buck converters. However, it should be noted that two primary windings of  $n_p$  turns each are required, and that they must be closely coupled magnetically. This causes the primary difficulty in constructing this transformer. The rms current in either transformer primary (or switch) is

$$i_{PRI}(rms) = i_{SW}(rms) = NI_o \sqrt{D_s} = \frac{I_s}{2\sqrt{D_s}} \quad (3.56)$$

Because there are two primary windings each having an rms current equal to that of the full-bridge divided by  $\sqrt{2}$ , 41% more copper is required for this transformer primary.

The switches in the push-pull circuit block a voltage

$$v_{sw} = 2V_s \quad (3.57)$$

assuming perfect coupling between the primary halves. The average switch current rating is:

$$i_{sw}(avg) = NI_o D_s = \frac{I_s}{2}. \quad (3.58)$$

Therefore, the expected conduction loss per switch, assuming ohmic switches, is:

$$P_{OHM} = (NI_o)^2 D_s R_{DS} = I_s^2 \frac{R_{DS}}{4D_s}. \quad (3.59)$$

The worst case for (3.59) occurs at low line, for which  $2D_s = 1.0$  and  $P_{DES} = I_s(max)V_s(min)$

$$\left. \frac{P_{OHM}}{P_{DES}} \right|_{wc} = \frac{1}{2} \frac{I_s(max)}{V_s(min)} R_{DS} \quad (3.60)$$

Assuming a blocking voltage of  $2V_s(max)$ , four devices could be paralleled to form two switches.

Using (3.1) as the model for an ohmic switch of a given die size ( $K$  is the same as for the full bridge), the following total conduction loss is obtained:

$$\begin{aligned} \left. \frac{P_{COND}}{P_{DES}} \right|_{wc} &= 2 \cdot \left[ \frac{1}{2} \frac{I_s(max)}{V_s(min)} \right] \cdot \frac{1}{2} [K(2V_s(max))^{2.5}] \\ &= 2\sqrt{2} I_s(max) K K_{TD} V_s^{1.5}(max) \end{aligned} \quad (3.61)$$

If four devices of the same size ( $K$  is the same) were seriesed to form two switches, the total conduction loss would be:

$$\left. \frac{P_{COND}}{P_{DES}} \right|_{wc} = 2 I_s(max) K K_{TD} V_s^{1.5}(max). \quad (3.62)$$

This result assumes ideal voltage sharing and can be seen to be the same as would be obtained in the full-bridge topology.

For constant-voltage-drop switches, the worst-case total conduction loss is:

$$\left. \frac{P_{COND}}{P_{DES}} \right|_{wc} = 2 K_{TD} \frac{V_{sw}}{2V_s(max)} \quad (3.63)$$

Blocking-voltage-related switching losses will be higher in the push-pull topology than in the full-bridge or half-bridge circuits. The peak switched current is the same as that of the full-bridge. Energy trapped in leakage fluxes which are coupled by both primary windings are returned to  $V_s$  in the same manner as in the full-bridge circuit. The minimum off-time given by (3.36) is need for currents related to this leakage flux to decay to zero. (In this equation,  $L_{ep}$  is interpreted as the primary-secondary leakage inductance referred to either primary half-winding.)

A major problem in applying the push-pull converter arises from imperfection in primary-primary coupling. Energy stored in this leakage flux produces a voltage overshoot on the blocking switch in the same manner as layout inductance, and it must either be dissipated (if dissipative snubbers are used) or recycled using more-complicated energy-recovering snubbers. This difficulty discourages the application of this topology at higher power levels.

### **Comparison of Buck Topologies**

The full-bridge form of the buck converter is favored by most designers for high-power designs. Therefore, it will be used as the standard for comparison with the half-bridge and push-pull circuits. The results of the previous sections are summarized in Tables 3.1 and 3.2.

Table 3.1 compares power circuit component sizing information for the three topologies. It is found that for given input-output ripple specifications, all three topologies store the same total energy in  $C_s$  and  $L_o$ . However, the half-bridge is disadvantaged by requiring two input capacitors, each rated for twice the rms current needed for the full-bridge input capacitor.

The push-pull topology requires a bigger transformer than the full-bridge. The VA product required is 21-percent greater due to the extra primary winding. The most severe practical limitation is probably the difficulty in closely coupling the two primary windings. Energy trapped in this leakage flux cannot be recycled without energy-recycling snubbers.

Table 3.2 compares the three topologies on the basis of switch ratings and expected conduction losses. The basis of comparison here is four devices of a given size which can be

paralleled or seriesed in an ideal manner. It is easily established that all three topologies have the same switch rating factor "R":

$$R_{rms} = R_{avg} = 2K_{TD}P_{DES},$$

where  $R_{rms}$  is defined to be the product of the total number of switches, their peak voltage rating and their rms current rating. The switch rating factor could also be defined in terms of the average switch current, producing the same result. If devices of a given type can be ideally paralleled, the conduction loss of the half-bridge topology is equal to that of the full-bridge. If devices of a given type could be ideally connected in series, the same would also be true of the push-pull topology. Seriesing is difficult, and should be avoided in practice, however. If ohmic devices obey the relation (3.1), then on-resistance increases with the 2.5 power of the voltage rating. Because of this, paralleling ohmic devices in the push-pull topology results in a 41-percent conduction loss penalty. Paralleling constant-voltage-drop devices in this topology may lower conduction losses, however.

If  $V_{SW}$  does not increase as much as linearly with blocking voltage, then the push-pull topology would have a conduction loss advantage. This may be useful with exceptionally low source voltages, where both ohmic and constant-voltage-drop devices tend to have resistance or voltage-drop dependent on die size and current density, but not voltage rating.

It seems clear that the full-bridge topology is favored for high power designs with good reason. Therefore, the design criterea obtained for the full-bridge buck topology will be compared with full-bridge versions of other converter types.

Table 3.1\ Buck Converter Topology Comparison

	Input Capacitor $C_s$	Output Inductor	Transformer
Full-Bridge	$C_s \geq \frac{P_{DES}}{\omega} \frac{2\pi}{27 R_V V_S^2(\min)}$ <p>RMS Current:  <math display="block">i_{rms} = \frac{1}{2} N I_o</math> Total Stored Energy:  <math display="block">E_{CS} = \frac{P_{DES}}{\omega} \frac{\pi K_{TD}}{27} \frac{(1 + R_V)^2}{R_V}</math></p>	$L_o \geq \frac{P_{DES}}{\omega} \frac{\pi}{2 R_I I_o^2(\max)} \frac{K_{TD}-1}{K_{TD}}$ <p>Total Stored Energy  <math display="block">E_{LO} = \frac{P_{DES}}{\omega} \frac{\pi}{4} \frac{K_{TD}-1}{K_{TD}} \frac{(1 + R_I)^2}{R_I}</math></p>	<p>Design Turns Ratio:  <math display="block">N \equiv \frac{n_s}{n_p} = \frac{V_o}{V_s(\min)}</math></p> <p>Volt-Second Integral:  <math display="block">VSI = \frac{V_o}{2fn_s}</math> Volt Ampere Product:  <math display="block">VSI \cdot \Sigma ni = \frac{P_{DES}}{f}</math></p>
Half-Bridge	<p>Need Two units, each <math>2C_s</math></p> <p>RMS current:  <math display="block">i_{rms} = N I_o</math> Total Stored Energy:  Same as FB</p>	Same as FB	Same as FB
Push-Pull	Same as FB	Same as FB	<p>N same as FB, but two primaries needed.</p> <p>VSI same as FB.</p> $VSI \cdot \Sigma ni = \frac{P_{DES}}{f} \frac{1 + \sqrt{2}}{2}$

Table 3.2. Buck Converter Topology Comparison

	Switch Rating (each)		Worst-Case Total Conduction Loss	
			(4 ohmic devices) die size " K11	(4 const-volt devices)
Full-Bridge	$V_{S(max)}$ (V peak)	$\frac{P_{DES}}{2V_{S(min)}}$ (A rms)	$\frac{P_{COND}}{P_{DES}} = 2I_S(max) K K_{TD} V_S^{1.5}(max)$	$\frac{P_{COND}}{P_{DES}} = 2 K_{TD} \frac{V_{SW}}{V_S(max)}$
	$\frac{P_{DES}}{2V_{S(min)}}$ (A avg)			
Half-Bridge	$V_S(max)$ (V peak)	$\frac{P_{DES}}{V_S(min)}$ (A rms)	Paralleled Devices:  Same as FB	Paralleled Devices:  Same as FB
	$\frac{P_{DES}}{V_S(min)}$ (A avg)			
Push-Pull	$2V_S(max)$ (V peak)	$\frac{P_{DES}}{2V_S(min)}$ (A rms)	Paralleled Devices: $\frac{P_{COND}}{P_{DES}} = 2\sqrt{2} I_S(max) K K_{TD} V_S^{1.5}(max)$	Paralleled Devices: $\frac{P_{COND}}{P_{DES}} = 2 K_{TD} \frac{V_{SW}}{2V_S(max)}$
	$\frac{P_{DES}}{2V_S(min)}$ (A avg)		Seriesed Devices: Same as FB	Seriesed Devices: Same as FB

## BOOST CONVERTER

A full-bridge boost converter is illustrated in Fig. 3.4, with idealized waveforms in Fig. 3.5. Half-bridge and push-pull implementations are also possible, but would not be advantageous at higher power levels for the reasons explored in the previous section on the buck converter; these are therefore not included here. Fig. 3.5 illustrates a set of drive waveforms which provide lowered conduction loss due to the fact that the inductor-charging interval is provided by turning on all switches simultaneously. This divides the source current between two parallel paths for a significant portion of the switching cycle. Alternate gating patterns are possible [23], such as the phase-shift pattern shown in Fig. 3.3 for the buck converter, but these produce the same net result. The phase-shift pattern does ease gate circuit design because of its fixed 50-percent duty cycle.

Perhaps the salient feature of Fig. 3.4 is the fact that the transformer is "current-fed," being supplied by an alternating current source with its secondary rectifier terminated "voltage-stiff" due to the large capacitor  $C_o$ . This is very beneficial in some ways. The tendency of the transformer core to "walk" up or down its B-H loop due to residual unbalance in the bridge switches is minimized by the impedance of  $L_s$  to sudden increases in transformer magnetizing current. The core walking problem can be a concern in the voltage-fed buck converters of Fig. 3.1, especially when square-loop core materials are used.

In the voltage-fed circuit, the core-walking problem is treated by air-gapping the transformer, or providing some type of feedback such as current-mode control [24]. Current-fed-transformer designs have a potentially serious drawback, however. Substantially low leakage inductance must be obtained in the transformer because the energy stored here causes a voltage spike at the switches when they turn off. This energy must be collected by the snubbers, either to be dissipated or recycled. The power efficiency tends to be impaired by this problem. (An experimental 2-kW 20-kHz converter built for this current research effort did not exceed 85 percent efficiency, primarily because of this problem.)



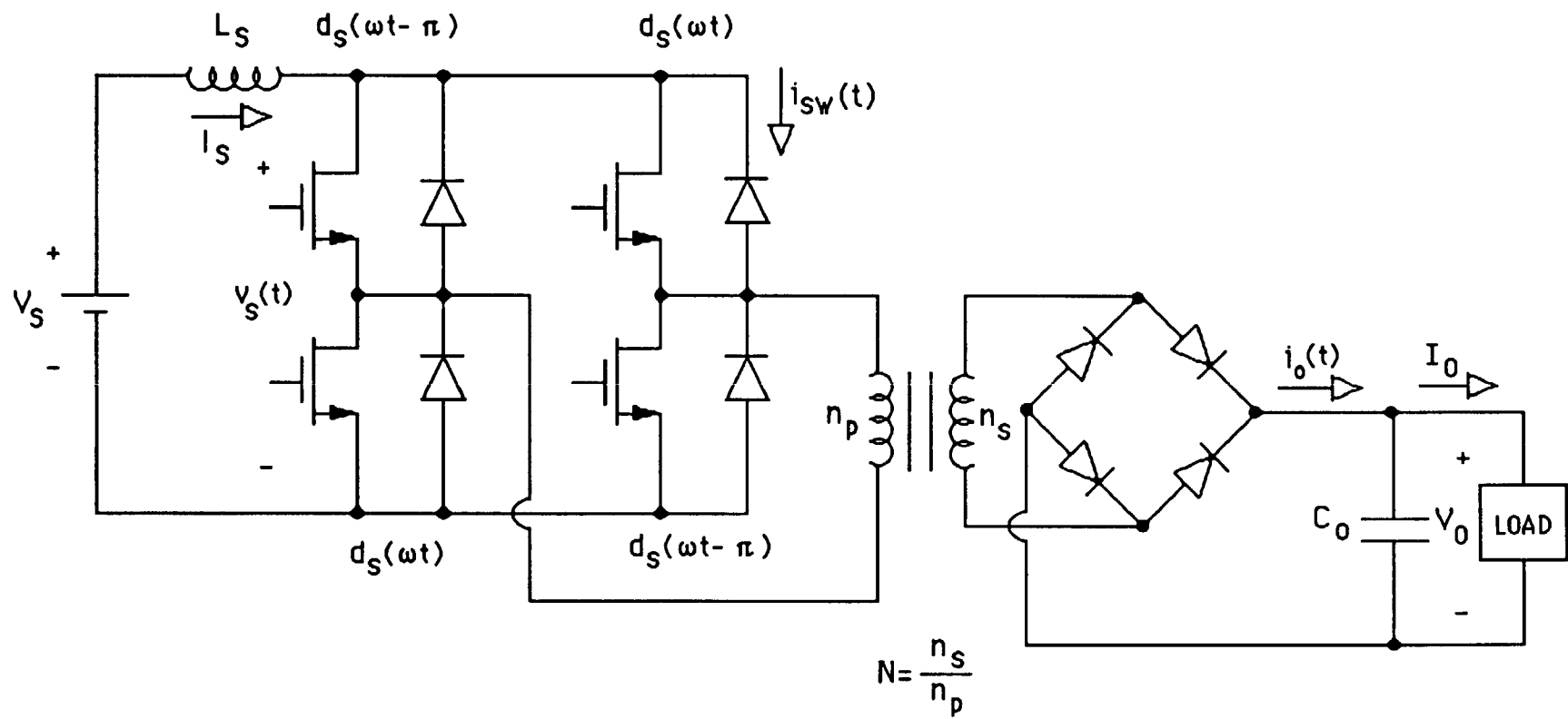


Fig. 3.4 Full-bridge boost converter.

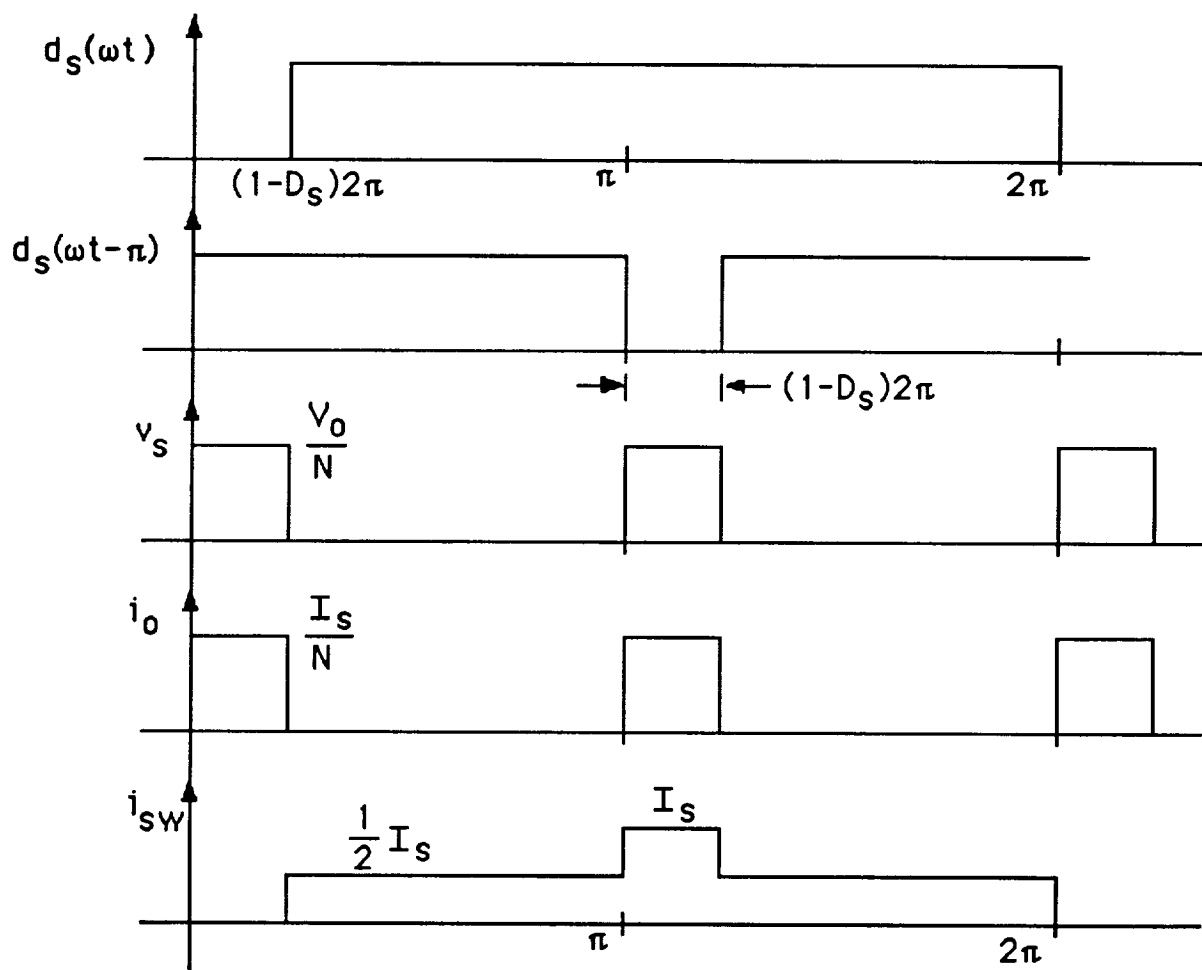


Fig. 3.5 Idealized waveforms for full-bridge boost converter.

### Full-Bridge Boost Converter

The analysis of the boost converter proceeds in a manner similar to that of the buck. The switch existence functions are given by (3.2) as before. The input voltage is:

$$\begin{aligned} v_s(\omega t) &= [1-d_s(\omega t)] \frac{V_o}{N} + [1-d_s(\omega t-\pi)] \frac{V_o}{N} \\ &= 2(1-D_s) \frac{V_o}{N} - \frac{4}{\pi} \frac{V_o}{N} \sum_{n=2}^{\infty} \frac{1}{n} \sin(n\pi D_s) \cos(n\omega t) \end{aligned} \quad (3.64)$$

for n even only.

The dc voltage transfer ratio is given by

$$V_o = \frac{NV_s}{2(1-D_s)} = \frac{NV_s}{2D'_s} \quad (3.65)$$

where

$$D'_s \equiv 1-D_s, \quad 0 \leq D'_s \leq 0.5. \quad (3.66)$$

The dominant unwanted component of  $V_s$  is the second harmonic. Its amplitude is:

$$|v_{s2}| = \frac{2V_o}{\pi N} \sin(2\pi D_s) \quad V_{\text{peak}} \quad (3.67)$$

Assuming that all of the ripple-voltage content of  $v_s$  is supported by  $L_s$ , its peak ripple current

$$|i_{sR}| = \frac{1}{2} \frac{1}{L_s} \int_0^{D_s} \left( \frac{V_o}{N} - 2D'_s \frac{V_o}{N} \right) dt$$

is found:

$$= \frac{V_o}{4NL_s f} (2D'_s)(1-2D'_s) \quad A_{\text{peak}} \quad (3.68)$$

The output current  $i_o$  is:

$$i_o(\omega t) = 2D'_s \frac{I_s}{N} - \frac{4}{\pi} \frac{I_s}{N} \sum_{n=2}^{\infty} \frac{1}{n} \sin(n\pi D_s) \cos n\omega t \quad (3.69)$$

for n even only.

The dominant unwanted component is the second harmonic. The rms value of  $i_o$  is readily found:

$$i_o(\text{rms}) = \frac{I_s}{N} \sqrt{2D'_s}. \quad (3.70)$$

Therefore, the rms ripple current in  $C_o$  is:

$$\begin{aligned} i_{oc}(\text{rms}) &= \frac{I_s}{N} \sqrt{2D'_s(1-2D'_s)} \\ &= I_o \sqrt{\frac{1-2D'_s}{2D'_s}} \end{aligned} \quad (3.71)$$

For a given output current  $I_o$ , the worst-case value of (3.71) occurs at the lowest  $D'_s$  within the operating range.

The ripple voltage appearing across  $C_o$  can be estimated by neglecting its ESR and assuming that all of the ripple current passes through it.

$$\begin{aligned} |v_{OR}| &= \frac{1}{2} \frac{1}{C_o} \int_0^{D'_s} \left( \frac{I_s}{N} - 2D'_s \frac{I_s}{N} \right) dt \\ &= \frac{I_s}{4C_o N f} (2D'_s)(1-2D'_s) \\ &= \frac{I_o}{4C_o f} (1-2D'_s) \quad V_{\text{peak}} \end{aligned} \quad (3.72)$$

There are normally additional contributions to this peak ripple voltage due to the capacitor ESL and ESR. These are a function of the style and quality of construction of  $C_o$ .

The transformer volt-second integral is:

$$VSI = \frac{V_o D'_s T}{n_s} \quad \text{V-sec} \quad (3.73)$$

where  $n_s$  is the number of secondary turns. The secondary winding current is

$$i_{SEC}(\text{rms}) = \frac{I_s}{N} \sqrt{2D'_s} = \frac{I_o}{\sqrt{2D'_s}} \quad \text{A rms.} \quad (3.74)$$

The product of the VSI and the total ampere-turns provides a measure of transformer size:

$$VSI \cdot \sum ni = \frac{V_o I_o}{f} \sqrt{2D'_s} \quad (3.75)$$

The transformer area product is readily calculated from (3.75) for a given flux density and current density, along with appropriate stacking and winding factors.

The switch ratings include a blocking voltage requirement of

$$v_{sw} = \frac{V_o}{N} \quad V_{peak} \quad (3.76)$$

The following current ratings are found from Fig. 3.5.

$$i_{sw}(avg) = \frac{1}{2} I_s \quad A_{avg} \quad (3.77)$$

and

$$i_{sw}(rms) = \frac{1}{2} I_s \sqrt{1+2D'_s} \quad A_{rms}. \quad (3.78)$$

The input inductor and output capacitor are chosen to meet specific ripple criteria.

Using the definition of current-ripple factor  $R_I$  given by (3.21), and using (3.68) and (3.69), the following design equation for  $L_s$  is found:

$$L_s = \frac{V_o}{4N^2 I_o R_I f} (2D'_s)^2 (1-2D'_s) \quad (3.79)$$

For a given output voltage and current, (3.79) maximizes for  $2D'_s = 2/3$ , giving:

$$L_s \geq \frac{V_o}{27 N^2 I_o R_I f} \quad (3.80)$$

The ripple factor increases when  $I_o$  is less than the design value (usually full load). The output capacitor is determined to meet a voltage ripple requirement  $R_v$ . Using (3.72):

$$C_o = \frac{I_o}{4C_o V_o f} (1-2D'_s) \quad (3.81)$$

This maximizes at the lowest value of  $2D'_s$  within the operating range. A suggested design procedure would be to set  $N$  using (3.65) and assuming  $2D'_s = 1$  at the maximum input voltage.

$$N = \frac{V_o}{V_s(max)} \quad (3.82)$$

The minimum value of  $2D'_s$  can then be found:

$$2D'_s(\min) = \frac{NV_s(\min)}{V_o} = \frac{1}{K_{TD}} \quad (3.83)$$

The required value of  $C_o$  is therefore:

$$C_o \geq \frac{I_o}{4R_V V_o f} \frac{K_{TD}-1}{K_{TD}} \quad (3.84)$$

The stored energies in  $L_s$  and  $C_o$  are calculated after the manner of (3.25)-(3.28) producing:

$$E_{LS} = \frac{P_{DES}}{\omega} \frac{\pi}{27} K_{TD}^2 \frac{(1+R_I)^2}{R_I} \text{ and} \quad (3.85)$$

$$E_{CO} = \frac{P_{DES}}{\omega} \frac{\pi}{4} \frac{K_{TD}-1}{K_{TD}} \frac{(1+R_I)^2}{R_V} \quad (3.86)$$

The conduction loss for each ohmic switch is estimated using (3.78), (3.65) and (3.82):

$$P_{OHM} = \left(\frac{I_s}{2}\right)^2 (1 + 2D'_s) R_{DS} = \frac{1}{4} \frac{P_{DES}^2}{V_s^2} \left(1 + \frac{V_s}{V_{s(\max)}}\right) R_{DS} \quad (3.87)$$

The design power is equal to the product of  $I_s(\max)$  and  $V_s(\min)$ . The worst case for (3.87) will occur at low line ( $V_s = V_s(\min)$ ):

$$\left. \frac{P_{OHM}}{P_{DES}} \right|_{wc} = \frac{1}{4} \frac{I_s(\max)}{V_s(\min)} \left(1 + \frac{1}{K_{TD}}\right) R_{DS} \quad (3.88)$$

The normalized conduction loss for all four ohmic switches, assuming they follow the model of (3.1), is found using (3.76) and (3.88):

$$\left. \frac{P_{COND}}{P_{DES}} \right|_{wc} = I_s(\max) K (1 + K_{TD}) V_s^{1.5}(\max) \quad (3.89)$$

The conduction loss for each constant-voltage-drop switch is found using (3.77):

$$\frac{P_{CV}}{P_{DES}} = \frac{I_s V_{sw}}{2I_s(\max) V_s(\min)} \quad (3.90)$$

The worst case for (3.90) occurs when  $I_s = I_s(\max)$ . For all four constant-voltage-drop switches the worst-case conduction loss is:

$$\left. \frac{P_{COND}}{P_{DES}} \right|_{wc} = 2 K_{TD} \frac{V_{sw}}{V_s(\max)} \quad (3.91)$$

The switching losses in the boost converter are related to the current interrupted and the voltage blocked, as always. However, the additional factors influencing these losses are quite different from those of the buck converter. At switch turn-on, current is commutated from the secondary-side rectifier to the incoming switch. Rectifier reverse-recovery-transient current may flow in the loop including the bridge switches, the transformer and capacitor  $C_o$ . The transformer leakage inductance will tend to control this transient current. The major difficulty with this circuit will be the voltage overshoot at switch turn-off caused by the transformer leakage inductance, which will invariably be much higher than the layout inductance achievable in the buck converter. Thus, a difficult trapped-energy problem may arise with this (or any current-fed) topology unless a low-leakage-flux design is possible for the transformer. The required blocking-voltage rating on the switches is likely to be much higher than  $V_s(\max)$ , therefore. Energy-recovering snubbers will be needed if significant leakage inductance exists in the transformer.

It is of interest to note that the buck converter (and all other voltage-fed topologies) provide a well-defined blocking voltage for their switches, if a low-inductance layout can be obtained. The topological dual, the boost converter (and all other current-fed topologies), provides a well-defined conduction current for its switches. The voltage-fed topologies are subject to transient currents at turn-on due to diode recovery. The current-fed topologies are subject to transient voltages at turn-off due to transformer leakage flux. Switching loss considerations probably tend to favor the boost, or other current-fed topologies, at low input voltages where over-rated switches are possible without on-resistance penalty, and low-leakage transformer design is easier.

## OTHER DC-DC CONVERTERS

The buck and boost converters have been studied in detail because they are basic; other dc-dc converters are generally derived from these and share their properties [23]. The Weinberg and TRW converters are next reviewed briefly.

### Weinberg Converter

Fig. 3.6 shows a full-bridge Weinberg converter [23]. Idealized operating waveforms are shown in Figs. 3.7 and 3.8. The salient features of this topology are its current-fed transformer, and its capability of operating as either a buck converter, or a boost converter.

Fig. 3.7 illustrates buck-mode operation. Switch existence functions are shown, with the restriction that their duty factors lie in the range  $0 \leq D_s \leq 0.5$ . When a set of bridge switches is closed, the inductor current  $I_s$  is coupled to the output through the transformer. Opening the bridge switches transfers the inductor current to its closely-coupled secondary, thus maintaining a continuous output current  $(i_1 + i_2)$  if the inductor turns ratio is set equal to the transformer turns ratio as assumed here. It is easy to establish that the ideal voltage and current transfer ratios are the same as those of the buck converter. One difference is found in the switch blocking voltage, which may be as high as twice the supply voltage in the buck mode. Also, the leakage inductance problems inherent to the current-fed transformer are compounded by the need to maintain close coupling on the inductor as well.



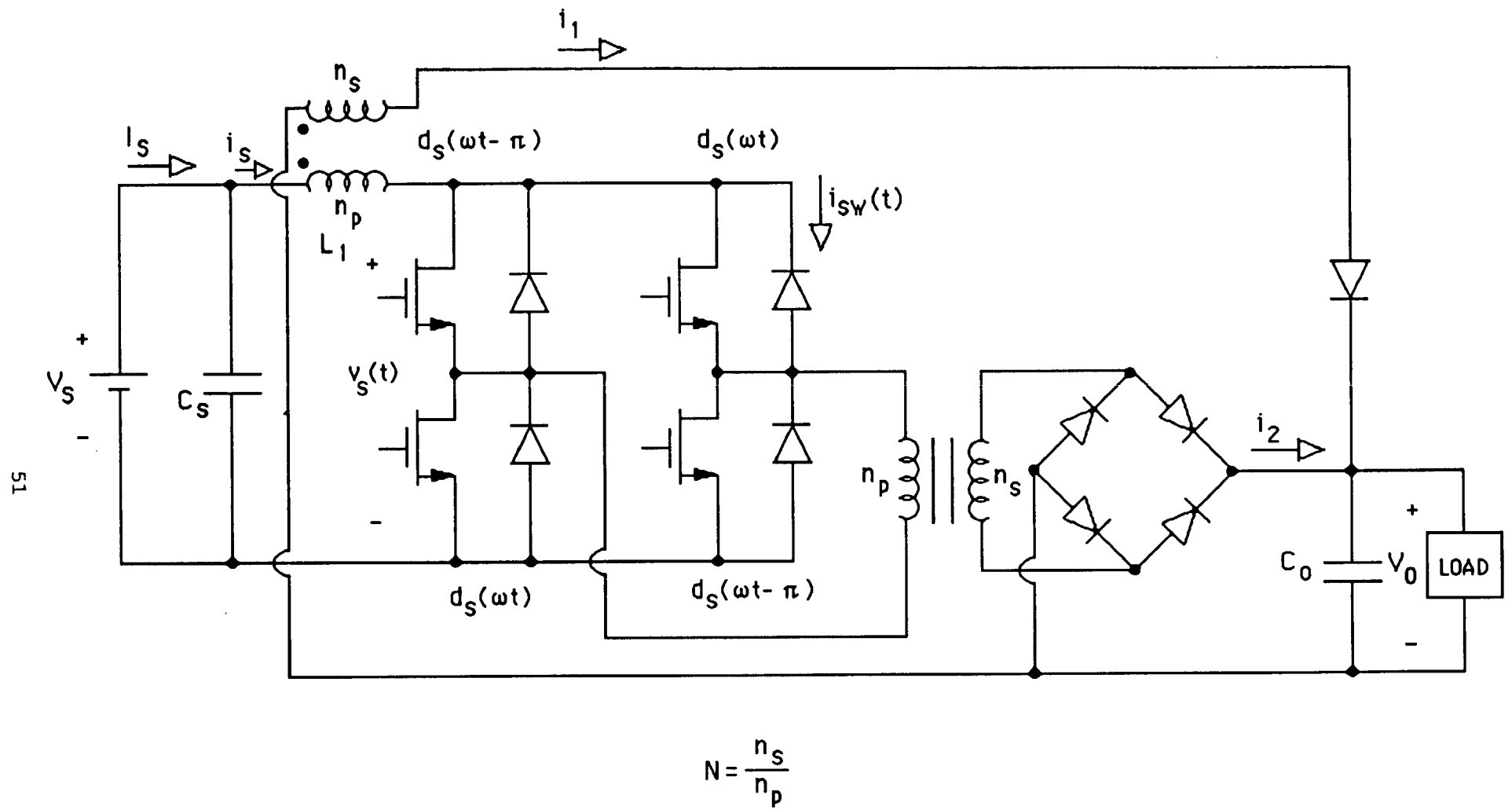
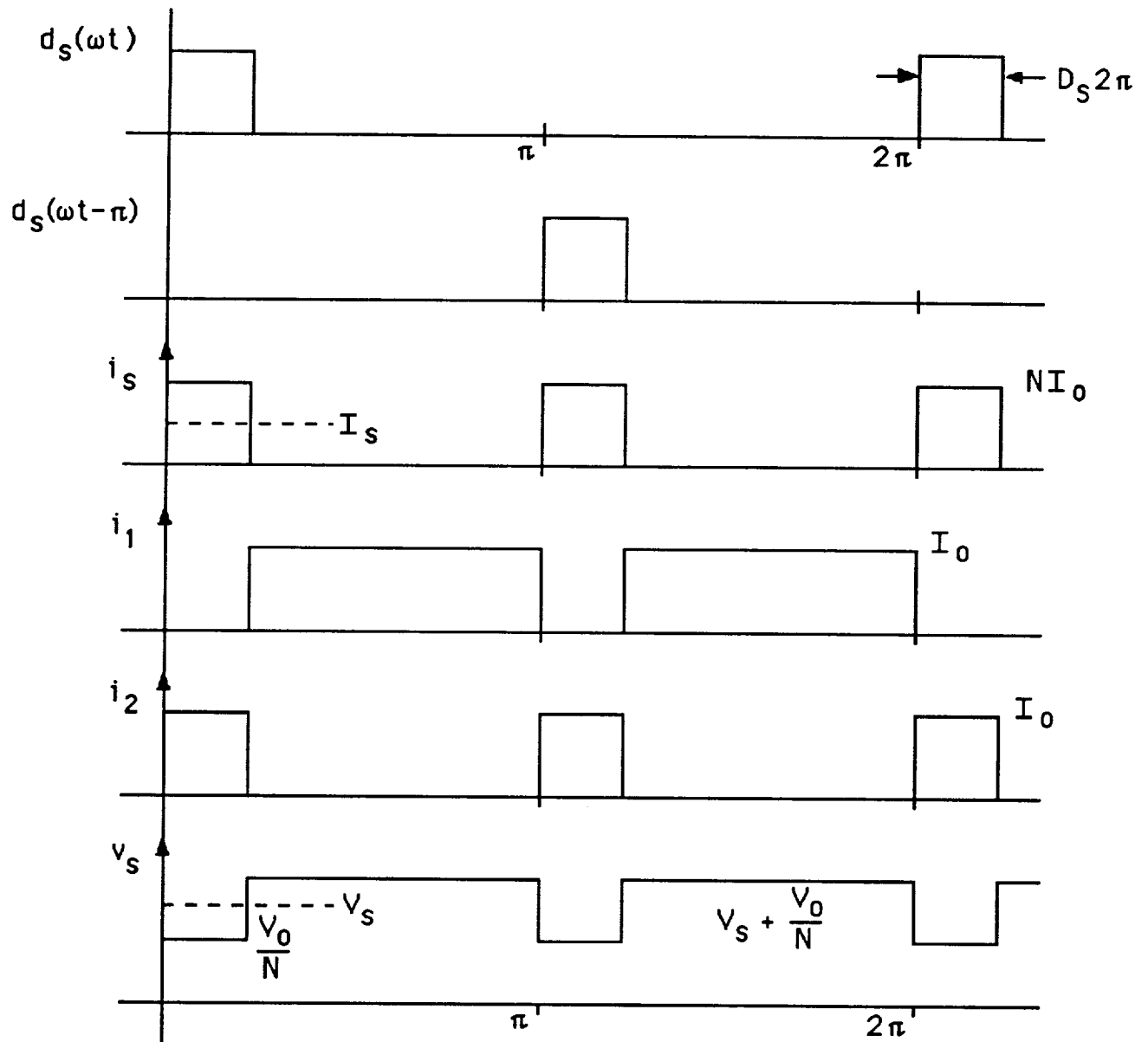


Fig. 3.6 Weinberg converter.

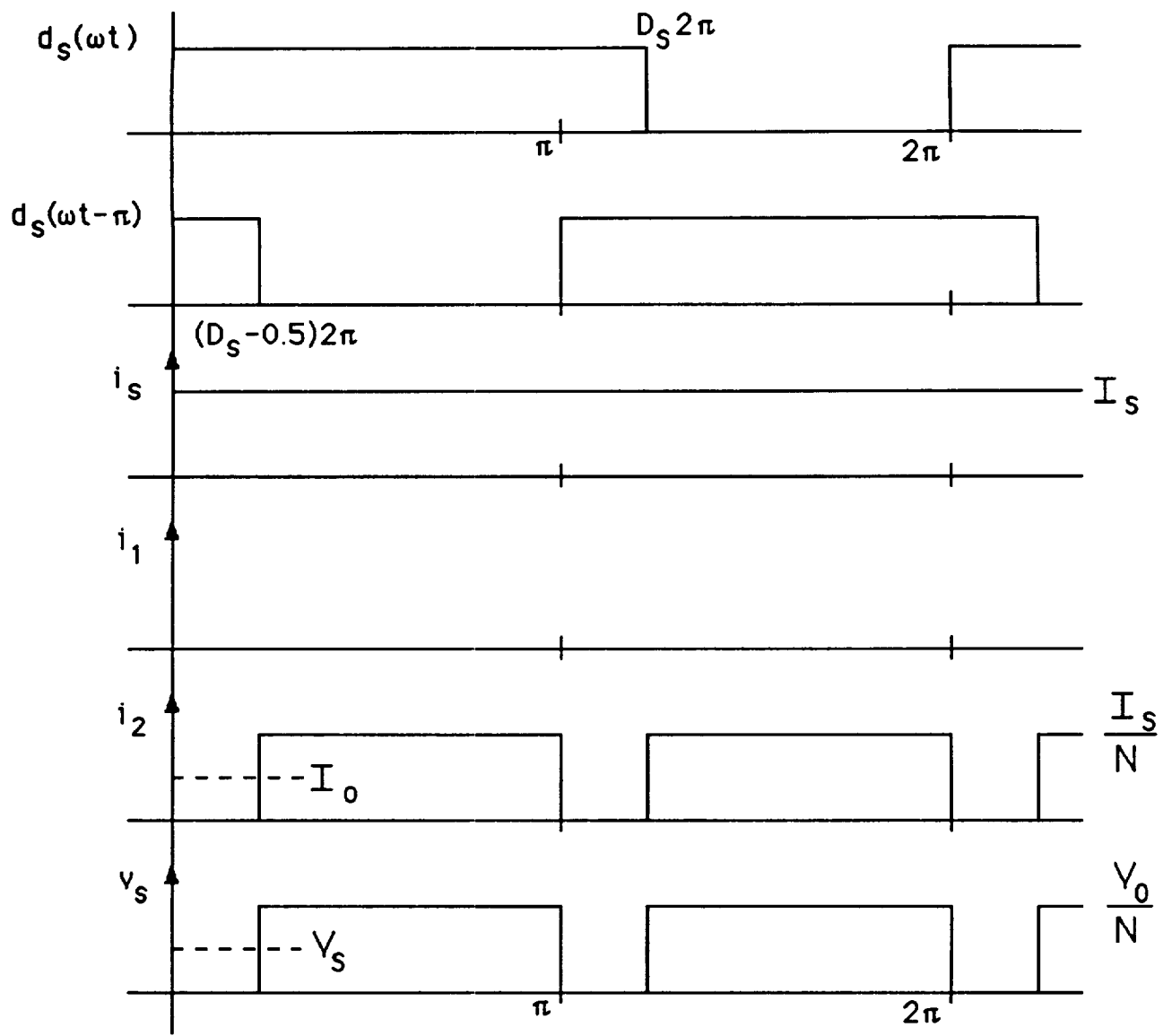


$$I_s = 2D_s NI_0$$

$$V_0 = 2D_s NV_s$$

$$0 \leq D_s \leq 0.5$$

Fig. 3.7 Weinberg converter operating in the buck mode.



$$I_0 = 2(1-D_s) \frac{I_s}{N} = 2D'_s \frac{I_s}{N}$$

$$V_s = 2D'_s \frac{V_0}{N}$$

$$0.5 \leq D_s < 1$$

Fig. 3.8 Weinberg converter operating in the boost mode.

The boost mode of the Weinberg converter is automatically entered when  $D_s$  exceeds 0.5. In this mode the input current  $i_s$  becomes continuous, the secondary of the inductor not being active. The circuit then operates the same as the boost converter discussed previously.

A buck-boost mode is also possible if all four bridge switches are operated in unison. The energy transfer would then be entirely through the inductor, the transformer not participating at all. This mode has no practical utility because buck and boost operation are already available.

The main attraction of this circuit would be its ability to operate as a boost converter under nominal conditions, but as a buck converter under fault conditions (such as load short-circuit). The boost converter has potentially lower conduction losses when ohmic devices are used (compare (3.34) with (3.89) ); however, it cannot operate with a load voltage lower than the reflected source voltage  $NV_s$ . The Weinberg circuit would permit normal operation in the boost mode, with start-up or short-circuit operation in the buck mode. This possibility was investigated experimentally on this grant and previously reported [14]. The converter worked as expected, but did not have notably high efficiency due to the snubbing losses associated with the imperfect coupling in the inductor and transformer. Another factor not yet considered here is the fact that in its buck mode the Weinberg converter exposes its switches to as much as  $2V_s(\text{max})$ . The boost-converter conduction-loss estimate of (3.89) is based on the ohmic switches rated for  $V_s(\text{max})$ . Therefore, for a given device die size, the boost-mode loss of the Weinberg converter would become  $2^{2.5}$  greater than that of the ordinary boost converter, thus erasing the potential gain. This converter is therefore not recommended for high-power application, except for the case of an unusually low source voltage.

### **TRW Converter**

Fig. 3.9 shows a TRW converter [23]. Here, the first switch operated with the existence function  $d_{s1}$  provides buck-mode PWM control of the output voltage. The bridge switches are operated with simple 50-percent duty cycles. The benefits (and liabilities) of a current-fed transformer are obtained in this circuit. As pointed out in [23], operation with a relatively small  $L_o$  can be used to lower the switching losses in the bridge switches--in the

discontinuous conduction mode the switching loss would be zero. However, the extra switches in the current path will result in increased conduction losses for this circuit, relative to a full-bridge buck converter. The TRW converter is shown here because it provides a means of exchanging switching losses for conduction losses, and for obtaining a current-fed transformer in a buck converter. However, it does not seem likely to offer any over all improvement on the basic buck converter, and is therefore not investigated further.

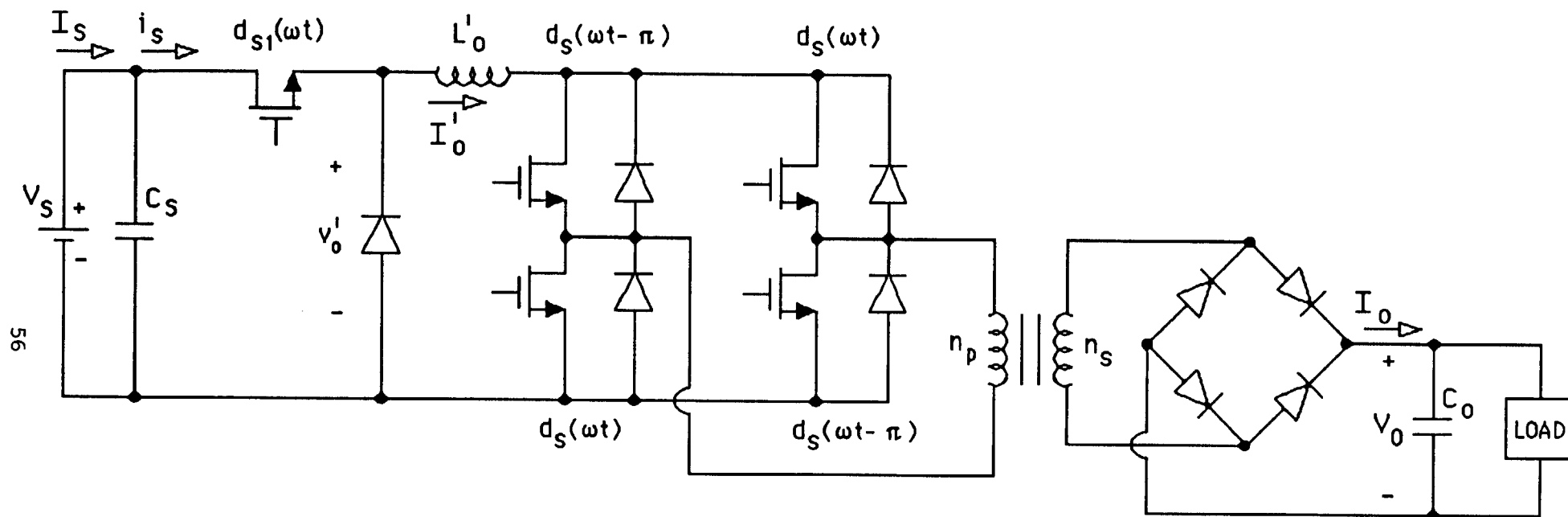


Fig. 3.9 TRW converter.

## SUMMARY OF SUGGESTED DESIGNS

Suggested designs for full-bridge buck and boost converters are summarized here for future reference. These designs are tabulated in Tables 3.3 and 3.4, along with expected worst-case conditions in the circuits. In both cases, transformer leakage flux is neglected in setting the turns ratio, as is switching device voltage-drop.

The boost converter is seen to have one potential advantage over the buck in the area of ohmic-switch conduction losses if large turn-down ratios are required. This advantage would be lost if tight coupling could not be achieved in the transformer, however. The major disadvantage of the boost converter, its inability to feed a faulted load, will eliminate it from further consideration for the application, however.

Likewise, the Weinberg converter has been eliminated due to its increased switch voltage, which negates the possible advantages of the boost mode unless operation down to a small fraction of the nominal input voltage is required. The TRW converter separates the buck converter from the transformer-feed switches, permitting a current-fed transformer. It is eliminated due to the extra conduction losses resulting. The transformer core-ratcheting problem is better solved in the control circuitry than in the power circuit.

The buck converter design of Table 3.3 is therefore carried forward for comparison with the resonant dc-dc converters.

Table 3.3 Full-Bridge Buck Converter Design Summary

Transformer	
-Turns Ratio	$N \equiv \frac{n_s}{n_p} = \frac{V_o}{V_s(\min)}$
-Volt-Second Integral	$VSI = \frac{V_o}{2fn_s}$
-VSI-Ampere Product	$VSI \cdot \Sigma ni = \frac{P_{DES}}{f}$
Duty Cycle Range	$\frac{1}{K_{TD}} \leq 2D_s^* \leq 1$ where $K_{TD} \equiv \frac{V_s(\max)}{V_s(\min)}$
Input Capacitor	
-Value	$C_s = \frac{P_{DES}}{V_s^2(\min)} \frac{1}{27 f R}$
-Ripple Current	$i_{cs}(\text{rms}) = 0.5 \frac{P_{DES}}{V_s(\min)}$
-Stored Energy	$E_{cs} = \frac{P_{DES}}{\omega} \frac{\pi}{27} K_{TD}^2 \frac{(1+R)^2}{R}$
Output Inductor	
-Value	$L_o = \frac{P_{DES}}{I_o^2} \frac{1}{4 f R} \frac{K_{TD}-1}{K_{TD}}$
-Stored Energy	$E_{LO} = \frac{P_{DES}}{\omega} \frac{\pi}{4} \frac{K_{TD}-1}{K_{TD}} \frac{(1+R)^2}{R}$
Conduction Losses	
-Four Ohmic + Devices	$\frac{P_{COND}}{P_{DES}} = 2 I_s(\max) K_{TD} K V_s^{1.5}(\max)$
-Four CV Devices	$\frac{P_{COND}}{P_{DES}} = 2 K_{TD} \frac{V_{SW}}{V_s(\max)}$

\*Effective duty cycle  $D = 2 D_s$

+  $R_{DS} = KV^{2.5}$



Table 3.4 Full-Bridge Boost Converter Design Summary

Transformer	
-Turns Ratio	$N \equiv \frac{n_s}{n_p} = \frac{V_o}{V_s(\min)}$
-Volt-Second Integral	$VSI = \frac{V_o}{2n_s}$
-VSI-Ampere Product	$VSI \cdot \Sigma ni = \frac{P_{DES}}{f}$
Duty Cycle Range	$\frac{1}{K_{TD}} \leq 2 D_s^* < 1$ where $K_{TD} \equiv \frac{V_s(\max)}{V_s(\min)}$
Input Inductor	
-Value	$L_s = \frac{V_s^2(\max)}{P_{DES}} \frac{1}{27 f R}$
-Stored Energy	$E_{LS} = \frac{P_{DES}}{\omega} \frac{\pi}{27} K_{TD}^2 \frac{(1+R)^2}{R}$
Output Capacitor	
-Value	$C_o = \frac{P_{DES}}{V_o^2} \frac{1}{4 f R} \frac{K_{TD}-1}{K_{TD}}$
-Ripple Current	$i_{co}(rms) = I_o \sqrt{K_{TD}-1}$
-Stored Energy	$E_{co} = \frac{P_{DES}}{\omega} \frac{\pi}{4} \frac{K_{TD}-1}{K_{TD}} \frac{(1+R)^2}{R}$
Conduction Losses	
-Four Ohmic + Devices	$\frac{P_{COND}}{P_{DES}} = 2 I_s(\max) (1+K_{TD}) K V_s^{1.5}(\max)$
-Four CV Devices	$\frac{P_{COND}}{P_{DES}} = 2 K_{TD} \frac{V_{sw}}{V_s(\max)}$
*Effective duty cycle $D = 1 - 2D_s^*$	
+ $R_{DS} = K V^{2.5}$	



#### IV. ANALYSIS OF RESONANT TOPOLOGIES

Much research effort has been expended on the resonant dc-dc and dc-ac converters in the past ten years. Claims made for various resonant topologies generally include higher switching frequency (for a given switching device), lower EMI and, sometimes, higher efficiency. These claims need to be examined critically in the light of the specific requirements of the problem at hand. The first claim, higher switching frequency, seems to be generally true. The various resonant converter eliminate switching losses on some of the switch's on-off transitions. The lowered switching loss, together with effective use of the transformer leakage inductance as a resonant circuit element, permits higher frequency. However, it is also invariably true that resonant converters suffer increased conduction losses, either due to multiplied switch currents (when zero-current-switching is obtained), or multiplied switch voltage (when zero-voltage-switching is obtained). The claim of higher efficiency is thus suspect, because the reduced switching loss of a resonant converter is obtained at the expense of increased conduction loss. It may be more accurate to claim higher efficiency at higher frequency. However, the highest attainable efficiency will probably be found by operating the topology having the lowest conduction loss at a low switching frequency. This approach will result in large bulk and weight, however. This chapter will review a variety of resonant dc-dc and dc-ac converters to characterize their expected conduction losses and component sizes for comparison with the non-resonant converters previously considered.

##### **SERIES-RESONANT INVERTER/CONVERTER**

The series-resonant converter [25, 26] is a useful higher-power dc-dc converter topology. An application of this to an ac distribution system in which the majority of the loads contain rectifiers has also been proposed [11, 12]. Because of the similarity of these two circuits, they will be considered together, either one being referred to as the "SRC." However, they are distinguished by variable-frequency or fixed-frequency operation.

Fig. 4.1 shows a full-bridge SRC. This is used as a dc-dc converter; control is by variation of the switching frequency relative to the resonant frequency. Either above- or

below-resonance operation may be selected. The switch duty cycle is fixed at 50 percent. Voltage-stiff interfaces are made at the input and output sides using capacitors  $C_s$  and  $C_o$ . In addition, significant resonant elements  $L$  and  $C$  are needed, plus a transformer to provide isolation and scaling.

Fig. 4.2 shows an ac distribution system established by an SRC having its ac link extended, and its load rectifier subdivided into multiple units for multiple loads. Because constant-frequency operation is probably a requirement for the ac distribution approach, the SRC is switched at a fixed frequency, with load regulation and short-circuit protection provided by the dc-dc converter of Fig. 4.2. This dc-dc converter may itself be an SRC as proposed in [11, 12], but other dc-dc converter topologies could be used as well. Load voltage scaling could be provided at each load by adding a high-frequency transformer, an advantage for this approach. However, the composite of all loads and load-bypass capacitors  $C_{OA}$ ,  $C_{OB}$ , . . . reflected back to the main transformer secondary should be equivalent to the single units shown in Fig. 4.1. The analysis of the ac-distribution portion of Fig. 4.2 is therefore the same as that of the SRC, with the exception of fixed-frequency operation. The analysis of the dc-dc converter portion of Fig. 4.2 is done separately, according to the topology selected for this use.

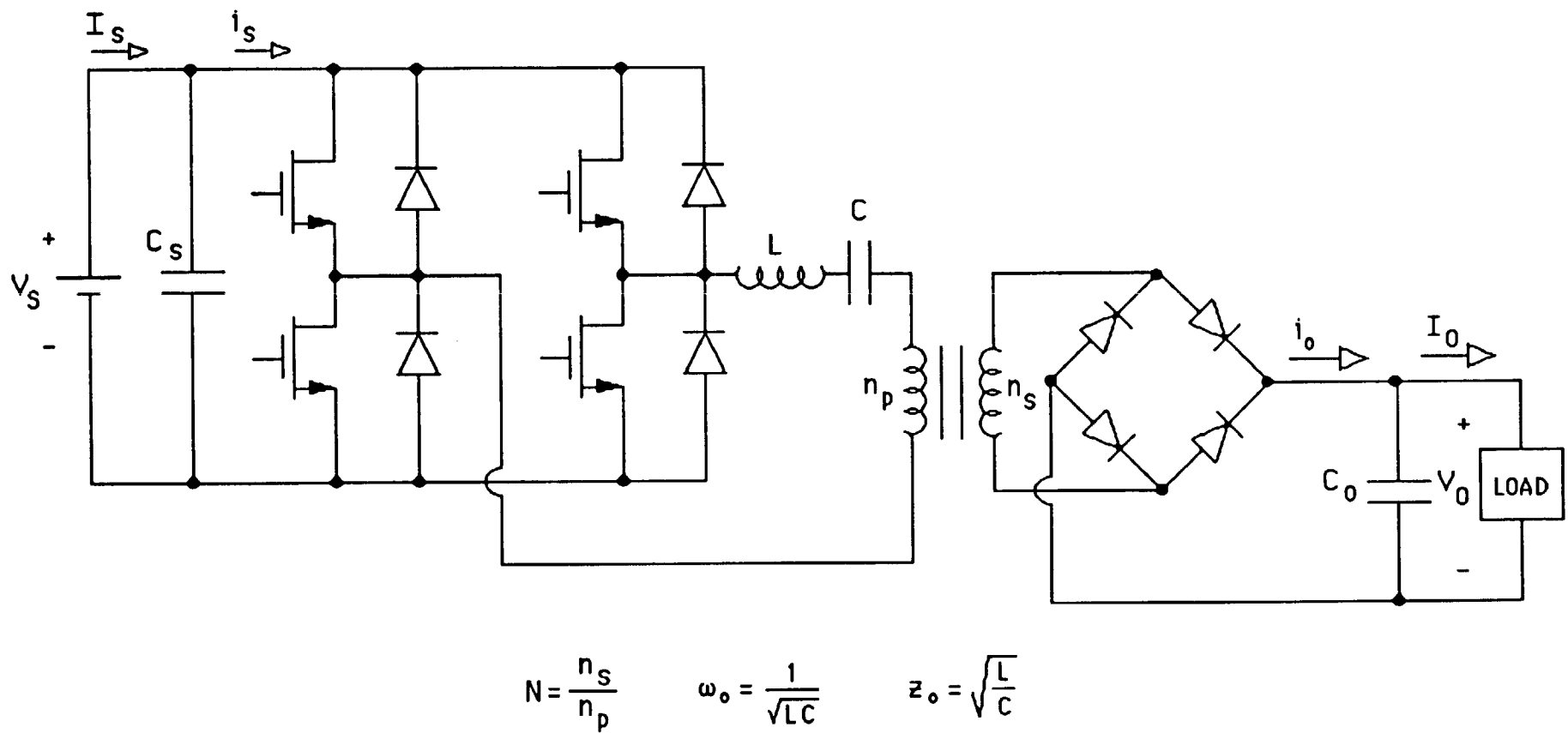
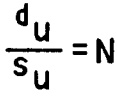


Fig. 4.1 Series-resonant dc-dc converter (SRC). Above- or below-resonance operation may be selected.



frequency is used.

### Variable-Frequency SRC Design and Performance

A useful design procedure for the SRC is found in [27]. This procedure attempts to minimize component stress (peak stored energy in the resonant tank, plus the peak switch current) while meeting design goals. The proposed procedure treats the resonant tank characteristic resistance ( $Z_o$ ) and the transformer turns ratio ( $N$ ) as design variables. The following design results and equations are taken from [27].

The recommended full-load design operating point of [27] is for below-resonance operation:

$$\begin{aligned} M &\equiv \frac{V_o}{NV_s} \cong 1 \quad \text{and} \\ J &\equiv \frac{NZ_o I_o}{V_s} \cong 1.4, \quad \text{where} \\ \omega_o &\equiv \frac{1}{\sqrt{LC}}, \quad Z_o \equiv \sqrt{\frac{L}{C}} \quad \text{and} \quad N \equiv \frac{n_s}{n_p}. \end{aligned} \quad (4.1)$$

The corresponding recommendation for above-resonance operation is:

$$\begin{aligned} M &\cong 0.95 \\ J &\cong 0.2 \end{aligned} \quad (4.2)$$

It is also concluded that above-resonance operation is preferable to below-resonance operation in terms of component stress. These recommendations will be directly applied to the SRC of Fig. 4.1 to develop a design procedure. For the constant-frequency SRC of Fig. 4.2 they must be modified to ensure adequate short-circuit-current limiting during the initial portion of the transient when  $C_s$  has not yet discharged.

The design procedure corresponding to (4.1) and (4.2) is next developed. For below-resonance continuous-conduction operation, the normalized output current-output voltage relationship is:

$$\begin{aligned} J &= \frac{2}{\gamma} \left\{ 1 + \sqrt{1 + (1-M^2)\tan^2 \frac{\gamma}{2}} \right\} \\ \text{where } \gamma &\equiv \frac{\pi\omega_o}{\omega}. \end{aligned} \quad (4.3)$$

The control variable  $\gamma$  is related to the switching frequency  $\omega$  as above. For above-resonance operation, the relationship is:

$$J = \frac{2}{\gamma} \left\{ 1 + \sqrt{1 + (1-M^2) \tan^2 \frac{\gamma}{2}} \right\} \quad (4.4)$$

For design purposes, it is useful to rewrite (4.3) and (4.4) as follows:

$$M = \sqrt{1 - \frac{(J \frac{\gamma}{2} \pm 1)^2 - 1}{\tan^2 \frac{\gamma}{2}}} \quad (4.5)$$

where the + is selected for above-resonance, and the - is selected for below-resonance. Because the desired value of  $M \cong 1$  can only be approached as a limiting case as  $\gamma$  approaches 180 degrees ( $\omega$  approaches  $\omega_0$ ), the proposed design procedure is to first identify how closely one is willing to approach the resonant frequency. Margin for controller imperfection must be maintained, because passing through resonance results in the unintended mode, and the reversal of the sign of the control transfer function.

The following suggested design values are to be applied at the minimum input voltage:

$$\begin{aligned} M &\leq M_{DES} = 0.95 \\ J &\leq J_{DES} = 0.2 \\ \frac{\omega}{\omega_0} &\geq 1.35 \end{aligned} \quad \text{(above resonance) (4.6)}$$

or

$$\begin{aligned} M &\leq M_{DES} = 0.90 \\ J &\leq J_{DES} = 1.4 \\ \frac{\omega}{\omega_0} &\leq 0.83 \end{aligned} \quad \text{(below resonance) (4.7)}$$



The required transformer turns ratio and tank characteristic resistance are found using (4.1).

$$\begin{aligned}
 N &= \frac{V_o}{M_{DES} V_s(\min)} \\
 &= 1.053 \frac{V_o}{V_s(\min)} && \text{(above resonance)} \\
 &= 1.111 \frac{V_o}{V_s(\min)} && \text{(below resonance)} \quad (4.8)
 \end{aligned}$$

$$\begin{aligned}
 Z_o &= M_{DES} J_{DES} \frac{V_s^2(\min)}{V_o I_o} \\
 &= 0.1900 \frac{V_s^2(\min)}{P_{DES}} && \text{(above resonance)} \\
 &= 1.260 \frac{V_s^2(\min)}{P_{DES}} && \text{(below resonance)} \quad (4.9)
 \end{aligned}$$

Once the desired switching frequency at design conditions is selected, the resonant frequency can be found using (4.6) and the design is fixed.

Peak capacitor voltage and peak inductor current are used to calculate peak stored energy in the resonant tank. The following normalized expressions are taken from [27]. For above-resonance operation:

$$J = \frac{M_{cp}}{\tan^{-1} \sqrt{\frac{(M_{cp} + 1)^2 - 1}{1 - M^2}}} \quad (4.10)$$

$$J = \frac{J_{LP} - 1 + M}{\tan^{-1} \sqrt{\frac{(J_{LP} + M)^2 - 1}{1 - M^2}}} \quad (4.11a)$$

$$\text{for } \frac{1 - M^2}{M} < J_{LP}$$

$$J = \frac{-1 + \sqrt{1 + \frac{J_{LP}^2}{1 - M^2}}}{\tan^{-1} \left[ \frac{J_{LP}}{1 - M^2} \right]} \quad (4.11b)$$

for  $\frac{1-M^2}{M} > J_{LP}$  .

For below-resonance operation:

$$J = \frac{M_{CP}}{\pi - \tan^{-1} \sqrt{\frac{(M_{CP} - 1)^2 - 1}{1 - M^2}}} \quad (4.12)$$

$$J = \frac{J_{LP} + 1 - M}{\pi - \tan^{-1} \sqrt{\frac{(J_{LP} - M)^2 - 1}{1 - M^2}}} \quad (4.13)$$

where the following normalized quantities are defined:

$$M_{CP} \equiv \frac{V_{CP}}{K_{TD} V_s(\min)} \quad (\text{peak capacitor voltage})$$

$$J_{LP} \equiv \frac{I_{LP} Z_o}{K_{TD} V_s(\min)} \quad (\text{peak inductor current})$$

$$M \equiv \frac{V_o}{NK_{TD} V_s(\min)} \quad (\text{output voltage})$$

$$J \equiv \frac{I_o Z_o}{NK_{TD} V_s(\min)} \quad (\text{output current}) .$$

An apparent typographical error has been corrected in (4.11b). It should be noted that the above normalization definitions allow for a variable supply voltage  $V_s = K_{TD} V_s(\min)$ , where  $K_{TD}$  is the turn-down ratio.

The peak stored energy in the resonant tank is calculated from the following:

$$\begin{aligned} E_{TANK} &= \frac{1}{2} L I_{LP}^2 + \frac{1}{2} C V_{CP}^2 \\ &= \frac{1}{2} \left[ \frac{Z_o}{\omega_o} \left( \frac{V_s J_{LP}}{Z_o} \right)^2 + \frac{1}{\omega_o Z_o} (V_s M_{CP})^2 \right] . \end{aligned} \quad (4.14)$$

Assuming that  $Z_o$  has been determined according to the design procedure (4.9), and that the normalized current and voltage values above are based on  $V_s(\min)$ , the tank energy is:

$$\begin{aligned} E_{TANK} &= \frac{P_{DES}}{\omega_o} \frac{J_{LP}^2 + M_{CP}^2}{2 (0.1900)} \quad (\text{above resonance}) \\ &\quad \text{or} \\ E_{TANK} &= \frac{P_{DES}}{\omega_o} \frac{J_{LP}^2 + M_{CP}^2}{2 (1.260)} \quad (\text{below resonance}) \end{aligned} \quad (4.15)$$

The rms value of the tank current can be found for the below-resonance case in [28]. The switch rms current is 70.7 percent of the tank rms current because of the half-wave symmetry known to exist in the SRC.

$$i_{sw}(rms) = \frac{i_{TANK}(rms)}{\sqrt{2}} \quad (4.16)$$

The average switch current is one-half the dc input current, the worst case occurring at low-line. Using (4.9):

$$\begin{aligned} i_{sw}(avg) &= \frac{1}{2} \frac{P_{DES}}{V_s(min)} \\ &= 0.095 \frac{V_s(min)}{Z_o} \quad (\text{above resonance}) \\ &= 0.630 \frac{V_s(min)}{Z_o} \quad (\text{below resonance}) \end{aligned} \quad (4.17)$$

The peak voltage and current appearing in the resonant tank are now calculated for the given full-load design conditions. Variable input voltage is assumed. Note that (4.3) - (4.13) must be solved numerically, being careful to enter using the actual supply voltage as the normalization base. The results are tabulated in Table 4.1, after returning to a normalization based on  $V_s(min)$ . It is interesting to note that the above-resonance design shows diminishing capacitor voltage with increasing input voltage, the load conditions constant at rated power. The inductor peak current rises 40 percent with doubling input voltage, however. It can also be seen that a below-resonance design has substantial increases in both the capacitor voltage and inductor current when the input voltage increases, the load being held constant. Tank energy is also indicated on Table 4.1, normalized with respect to the power level and resonant frequency. It can be seen that the worst-case for stored energy occurs at high line, as might be expected.

Table 4.2 displays switch rating information and conduction losses for the full-power operating conditions of Table 4.1. The  $\alpha$  angles corresponding to the below-resonance entries on Table 4.2 are given to permit consulting [28], from which the indicated rms tank currents were obtained. The rms tank current for the above-resonance design was estimated, assuming

that the current has the same peak-to-rms ratio as a sinusoid. The conduction losses for four ohmic switches can be found from:

$$\frac{P_{COND}}{P_{DES}} = \frac{4}{P_{DES}} \cdot I_{SW}^2 (rms) \cdot K V_S^{2.5} (max) . \quad (4.18)$$

This expression should be evaluated under the conditions resulting in the highest switch current.

Table 4.1 Variable-Frequency Series-Resonant-Converter Design  
(Resonant Tank Stress)

	$V_s = V_s(\min)$	$V_s = 1.5 V_s(\min)$	$V_s = 2.0 V_s(\min)$
Above Resonance Design	$\frac{\omega}{\omega_o} = 1.352$ $Z_o = 0.19 V_s^2(\min)/P_{DES}$ $V_o = 0.95 N V_s(\min)$ $I_o N Z_o = 0.2 V_s(\min)$ $V_{cp} = 0.23 V_s(\min)$ $I_{LP} = 0.28 \frac{V_s(\min)}{Z_o} = 1.49 \frac{P_{DES}}{V_s(\min)}$ $E_{TANK} = 0.35 P_{DES}/\omega_o$ $= 0.48 P_{DES}/\omega$	$\frac{\omega}{\omega_o} = 3.854$ $V_o = \text{same}$ $I_o = \text{same}$ $V_{cp} = 0.082 V_s(\min)$ $I_{LP} = 0.39 \frac{V_s(\min)}{Z_o} = 2.04 \frac{P_{DES}}{V_s(\min)}$ $E_{TANK} = 0.41 P_{DES}/\omega_o$	$\frac{\omega}{\omega_o} = 6.267$ $V_o = \text{same}$ $I_o = \text{same}$ $V_{cp} = 0.050 V_s(\min)$ $I_{LP} = 0.40 \frac{V_s(\min)}{Z_o} = 2.09 \frac{P_{DES}}{V_s(\min)}$ $E_{TANK} = 0.42 P_{DES}/\omega_o$
Below Resonance Design	$\frac{\omega}{\omega_o} = 0.830$ $Z_o = 1.26 V_s^2(\min)/P_{DES}$ $V_o = 0.90 N V_s(\min)$ $I_o N Z_o = 1.4 V_s(\min)$ $V_{cp} = 2.65 V_s(\min)$ $I_{LP} = 2.55 \frac{V_s(\min)}{Z_o} = 2.02 \frac{P_{DES}}{V_s(\min)}$ $E_{TANK} = 5.36 P_{DES}/\omega_o$ $= 4.45 P_{DES}/\omega$	$\frac{\omega}{\omega_o} = 0.6545$ $V_o = \text{same}$ $I_o = \text{same}$ $V_{cp} = 3.36 V_s(\min)$ $I_{LP} = 2.76 \frac{V_s(\min)}{Z_o} = 2.19 \frac{P_{DES}}{V_s(\min)}$ $E_{TANK} = 7.50 P_{DES}/\omega_o$	$\frac{\omega}{\omega_o} = 0.5429$ $V_o = \text{same}$ $I_o = \text{same}$ $V_{cp} = 4.05 V_s(\min)$ $I_{LP} = 2.95 \frac{V_s(\min)}{Z_o} = 2.34 \frac{P_{DES}}{V_s(\min)}$ $E_{TANK} = 9.97 P_{DES}/\omega_o$

Table 4.2 Variable-Frequency Series-Resonant-Converter Design  
(Switch Stress and Conduction Loss)

	$V_s = V_s(\min)$	$V_s = 1.5V_s(\min)$	$V_s = 2.0 V_s(\min)$
Above Resonance Design	$\frac{\omega}{\omega_o} = 1.352$ See also Table 3.1 $I_{TANK} \cong 0.20 \frac{V_s(\min)}{Z_o}$ (A rms) $I_{SW} \cong 0.14 \frac{V_s(\min)}{Z_o}$ (A rms) $I_{SW} \cong 0.095 \frac{V_s(\min)}{Z_o}$ (A avg) $\frac{P_{COND}}{P_{DES}} = 2 \frac{V_{SW}}{V_s(\min)}$ (const.-volt-drop)	$\frac{\omega}{\omega_o} = 3.854$ $I_{TANK} \cong 0.28 \frac{V_s(\min)}{Z_o}$ (A rms) $I_{SW} \cong 0.20 \frac{V_s(\min)}{Z_o}$ (A rms) $I_{SW} = 0.063 \frac{V_s(\min)}{Z_o}$ (A avg)	$\frac{\omega}{\omega_o} = 6.267$ $I_{TANK} \cong 0.28 \frac{V_s(\min)}{Z_o}$ (A rms) $I_{SW} \cong 0.20 \frac{V_s(\min)}{Z_o}$ (A rms) $I_{SW} \cong 0.048 \frac{V_s(\min)}{Z_o}$ (A avg) $\frac{P_{COND}}{P_{DES}} \cong 4.4 I_S(\max) K_{TDK} V_S^{1.5}(\max)$ (ohmic)
Below Resonance Design	$\frac{\omega}{\omega_o} = 0.830$ See also Table 3.1 $I_{TANK} = 1.65 \frac{V_s(\min)}{Z_o}$ (A rms) $I_{SW} = 1.17 \frac{V_s(\min)}{Z_o}$ (A rms) $I_{SW} = 0.63 \frac{V_s(\min)}{Z_o}$ (A avg) $\frac{P_{COND}}{P_{DES}} = 3.45 I_S(\max) K_{TDK} V_S^{1.5}(\max)$ (ohmic) $\frac{P_{COND}}{P_{DES}} = 2 \frac{V_{SW}}{V_s(\min)}$ (const.-volt-drop)	$\frac{\omega}{\omega_o} = 0.6545$ $\alpha = 114^\circ$ $I_{TANK} \cong 1.62 \frac{V_s(\min)}{Z_o}$ (A rms) $I_{SW} = 1.15 \frac{V_s(\min)}{Z_o}$ (A rms) $I_{SW} = 0.42 \frac{V_s(\min)}{Z_o}$ (A avg)	$\frac{\omega}{\omega_o} = 0.5429$ $\alpha = 159^\circ$ $I_{TANK} \cong 1.60 \frac{V_s(\min)}{Z_o}$ (A rms) $I_{SW} = 1.13 \frac{V_s(\min)}{Z_o}$ (A rms) $I_{SW} = 0.32 \frac{V_s(\min)}{Z_o}$ (A avg)

\*Estimated

For below resonance operation, the worst-case of (4.18) occurs at low-line. Using (4.9),

$$\left. \frac{P_{COND}}{P_{DES}} \right|_{wc} = 3.45 I_S (\max) K_{TD} K V_S^{1.5} (\max) \quad (\text{below resonance}) \quad (4.19)$$

where  $I_S (\max) = P_{DES} / V_S (\min)$  .

For above-resonance operation, the worst-case occurs at high-line:

$$\left. \frac{P_{COND}}{P_{DES}} \right|_{wc} = 4.4 I_S (\max) K_{TD} K V_S^{1.5} (\max) \quad (\text{above resonance}) \quad (4.20)$$

where  $I_S (\max)$  is interpreted the same as before. The above-resonance conduction losses seem to drop at low-line. Because of the error possible in the estimated rms switch current, the difference between (4.19) and (4.20) is probably not significant. The total conduction loss for four constant-voltage-drop devices is found using (4.17):

$$\frac{P_{COND}}{P_{DES}} = 2 \frac{V_{SW}}{V_S (\min)} \quad (4.21)$$

This applies both above and below resonance. The results of (4.19) - (4.21) are entered on Table 4.2 in the columns representing their worst-cases.

### Fixed-Frequency SRC Design and Performance

The ac-distribution system illustrated in Fig. 4.2 contains a fixed-frequency SRC with its ac link extended to a multiplicity of paralleled loads. Because the majority of the anticipated loads will need filtered dc, simple rectifiers of the type shown are assumed at each load. The composite effect of all loads is much the same as that of the single load of Fig. 4.1. Fixed-frequency operation is desirable in a distribution system. Therefore, regulation and steady-state fault-current control is done by the dc-dc converter of Fig. 4.2. However, transient fault currents must be managed by the SRC itself, acting without the benefit of a controller. This is especially true if the fault is a low-resistance short. In this case, the SRC must limit the fault current to an acceptable level as  $C_s$  discharges, a process which could easily take long enough for the SRC to find a new steady-state as the charge in  $C_s$  decays. (The energy in  $C_s$  is only dissipated by the internal losses in the SRC during a fault.)

Although it is not shown in Fig. 4.2, a rectifier feeding  $C_s$  from the bus should be provided in case of an open-circuit fault. This rectifier normally would be inactive, but would limit the transient ac voltage and recycle the energy stored in the resonant tank in case of an open-circuit fault.

The previous design equations are now used to explore an SRC design with inherent fault-current limiting. For this purpose, the ratio of fault current to design full-load current is calculated using (4.3) and 4.4):

$$\frac{I_o(SC)}{I_o(DES)} = \frac{J_{SC}}{J_{DES}} = \frac{2 \left\{ \pm 1 + \sqrt{1 + \tan^2 \frac{\gamma}{2}} \right\}}{J_{DES}} \quad (4.22)$$

where the - is selected for above-resonance and the + is selected for below-resonance operation. In the application of (4.22), the input voltage is assumed to be regulated at its design value by the dc-dc converter. The suggested design conditions of Table 4.1



were checked using (4.22). Above-resonance operation ( $\omega/\omega_o = 1.352$ ,  $M_{DES} = 0.95$ ,  $J_{DES} = 0.2$ ) was found to result in a short-circuit current ratio of 6.5; below-resonance operation ( $\omega/\omega_o = 0.830$ ,  $M_{DES} = 0.90$ ,  $J_{DES} = 1.4$ ) was found to result in a short-circuit current a ratio of 1.6. It is apparent that above-resonance operation near the minimum stress point of [27] will require an additional current-limiting feedback, with its concomitant shift in switching frequency during fault conditions. This complication is probably not acceptable, therefore the above-resonance design approach will require a shift away from the optimum design of [27] to achieve satisfactory inherent current limiting. The below-resonance fault current of 1.6 times design current is probably acceptable, because it only occurs under fault conditions, and does not continue indefinitely.

Appropriate designs for above-resonance operation with 2 : 1 short-circuit-current limiting were investigated. Sample designs are shown on Table 4.3. Three possible designs ("A", "B" and "C") are shown with their corresponding full-load and short-circuit component stresses. All exhibit an output-side short-circuit current two times the full-load current. It can be seen that the normalized load voltage  $M_{DES}$  has to be lower than optimum to achieve current limiting. Comparison of Table 4.3 with the  $V_s = V_{s(min)}$  entry on Table 4.1 shows that short-circuit-current limiting is obtained at the price of increased switch current and stored energy at full-load conditions.

Table 4.3 Fixed-Frequency SRC Design, Above Resonance  
(Inherent 2 : 1 Short-Circuit-Current Limiting)

	Design A $J_{DES} = 0.2, M_{DES} = 0.7275$	Design B $J_{DES} = 0.6, M_{DES} = 0.7755$	Design C $J_{DES} = 0.1, M_{DES} = 0.7135$
Design	$\omega_o = \frac{\omega}{2.391}$ $Z_o = 0.1455 \frac{V_s^2}{P_{DES}}$ $N = 1.375 \frac{V_o}{V_s}$	$\omega_o = \frac{\omega}{1.386}$ $Z_o = 0.4653 \frac{V_s^2}{P_{DES}}$ $N = 1.289 \frac{V_o}{V_s}$	$\omega_o = \frac{\omega}{4.173}$ $Z_o = 0.07135 \frac{V_s^2}{P_{DES}}$ $N = 1.402 \frac{V_o}{V_s}$
Full-Load Stresses	$V_{CP} = 0.1314 V_s$ $I_{LP} = 0.3631 \frac{V_s}{Z_o} = 2.50 \frac{P_{DES}}{V_s}$ $E_{TANK} = 0.51 \frac{P_{DES}}{\omega_o} = 1.2 \frac{P_{DES}}{\omega}$	$V_{CP} = 0.6800 V_s$ $I_{LP} = 0.9045 \frac{V_s}{Z_o} = 1.94 \frac{P_{DES}}{V_s}$ $E_{TANK} = 1.38 \frac{P_{DES}}{\omega_o} = 1.91 \frac{P_{DES}}{\omega}$	$V_{CP} = 0.03764 V_s$ $I_{LP} = 0.1940 \frac{V_s}{Z_o} = 2.72 \frac{P_{DES}}{V_s}$ $E_{TANK} = 0.27 \frac{P_{DES}}{\omega_o} = 1.14 \frac{P_{DES}}{\omega}$
Short-Circuit Stresses	$V_{CP} = 0.2627 V_s$ $I_{LP} = 0.7710 \frac{V_s}{Z_o} = 5.30 \frac{P_{DES}}{V_s}$ $E_{TANK} = 2.28 \frac{P_{DES}}{\omega_o} = 5.45 \frac{P_{DES}}{\omega}$ $I_o(sc) = 2 I_o (DES)$	$V_{CP} = 1.3600 V_s$ $I_{LP} = 2.137 \frac{V_s}{Z_o} = 4.59 \frac{P_{DES}}{V_s}$ $E_{TANK} = 6.90 \frac{P_{DES}}{\omega_o} = 9.56 \frac{P_{DES}}{\omega}$ $I_o(sc) = 2 I_o (DES)$	$V_{CP} = 0.07528 V_s$ $I_{LP} = 0.3953 \frac{V_s}{Z_o} = 5.54 \frac{P_{DES}}{V_s}$ $E_{TANK} = 1.14 \frac{P_{DES}}{\omega_o} = 4.74 \frac{P_{DES}}{\omega}$ $I_o(sc) = 2 I_o (DES)$

Table 4.4 Fixed-Frequency SRC Design, Below Resonance  
(Inherent 2:1 Short-Circuit-Current Limiting)

	Design D J <sub>DES</sub> = 1.4, M <sub>DES</sub> = 0.9549	Design E J <sub>DES</sub> = 2.0, M <sub>DES</sub> = 0.9223	Design F J <sub>DES</sub> = 1.2, M <sub>DES</sub> = 0.9759
Design	$\omega_o = \frac{\omega}{0.8641}$ $Z_o = 1.337 \frac{V_s^2}{P_{DES}}$ $N = -1.047 \frac{V_o}{V_s}$	$\omega_o = \frac{\omega}{0.9030}$ $Z_o = 1.845 \frac{V_s^2}{P_{DES}}$ $N = -1.084 \frac{V_o}{V_s}$	$\omega_o = \frac{\omega}{0.8431}$ $Z_o = 1.171 \frac{V_s^2}{P_{DES}}$ $N = -1.025 \frac{V_o}{V_s}$
Full-Load Stresses	$V_{CP} = 2.545 V_s$ $I_{LP} = 2.500 \frac{V_s}{Z_o} = 1.87 \frac{P_{DES}}{V_s}$ $E_{TANK} = 4.76 \frac{P_{DES}}{\omega_o} = 4.11 \frac{P_{DES}}{\omega}$	$V_{CP} = 3.479 V_s$ $I_{LP} = 3.401 \frac{V_s}{Z_o} = 1.84 \frac{P_{DES}}{V_s}$ $E_{TANK} = 6.42 \frac{P_{DES}}{\omega_o} = 5.79 \frac{P_{DES}}{\omega}$	$V_{CP} = 2.236 V_s$ $I_{LP} = 2.211 \frac{V_s}{Z_o} = 1.89 \frac{P_{DES}}{V_s}$ $E_{TANK} = 4.22 \frac{P_{DES}}{\omega_o} = 3.56 \frac{P_{DES}}{\omega}$
Short-Circuit Stresses	$V_{CP} = 5.089 V_s$ $I_{LP} = 4.089 \frac{V_s}{Z_o} = 3.06 \frac{P_{DES}}{V_s}$ $E_{TANK} = 15.94 \frac{P_{DES}}{\omega_o} = 13.77 \frac{P_{DES}}{\omega}$ $I_o(sc) = 2I_o(DES)$	$V_{CP} = 6.955 V_s$ $I_{LP} = 5.955 \frac{V_s}{Z_o} = 3.23 \frac{P_{DES}}{V_s}$ $E_{TANK} = 22.72 \frac{P_{DES}}{\omega_o} = 20.52 \frac{P_{DES}}{\omega}$ $I_o(sc) = 2I_o(DES)$	$V_{CP} = 4.471 V_s$ $I_{LP} = 3.471 \frac{V_s}{Z_o} = 2.96 \frac{P_{DES}}{V_s}$ $E_{TANK} = 13.68 \frac{P_{DES}}{\omega_o} = 11.53 \frac{P_{DES}}{\omega}$ $I_o(sc) = 2I_o(DES)$

Table 4.4 summarizes the component stresses for three below-resonance designs having a 2 : 1 short-circuit-current ratio. As seen in Tables 4.1 and 4.2, below-resonance operation generally requires more total stored energy in the tank than above-resonance designs. This increase is primarily due to the high capacitor voltage found in below-resonance designs -- the corresponding inductor (and switch) currents are somewhat lower. Below-resonance designs having good short-circuit-current limiting are generally close to the optimum full-load design, and control peak switch currents substantially better than equivalent above-resonance designs. They require much higher-voltage, higher-energy capacitors, and have much greater total stored energy than above-resonance designs, however. Appropriate above-resonance designs are somewhat removed from the full-load optimum. However, they still have much lower total stored energy in their tanks.

The choice between above- and below- resonance operation of the fixed-frequency SRC should consider two factors: (1) the capacitor voltage and stored energy, and (2) the peak switch current under short-circuit conditions. The below-resonance design does a better job of limiting the peak current, while the above-resonance design does a better job of controlling the peak stored energy, especially in the capacitor. Design A of Table 4.3 is brought forth as a good above-resonance design. Although designs D-F of Table 4.4 have been given to provide direct comparisons with designs A-C, it is now seen that the "optimum" variable-frequency design of Tables 4.1 and 4.2 is also best for fixed frequency. The short-circuit performance of this design is therefore studied on Table 4.5. Design G (below-resonance) is seen to have a peak tank current of  $2.02 P_{DES}/V_s$  at full-load with a stored energy of  $4.45 P_{DES}/\omega$ .

Table 4.5 Short-Circuit Performance of a  
Proposed Below-Resonance Design

	Design G (See also Tables 4.1 and 4.2) JDES = 1.4, MDES = 0.90
Design (See also Tables 4.1 and 4.2)	$\omega_o = \frac{\omega}{0.830}$ $Z_o = 1.260 \frac{V_s^2}{P_{DES}}$ $N = 1.111 \frac{V_o}{V_s}$
Full-Load Stresses	$V_{cp} = 2.649 V_s$ $I_{LP} = 2.549 \frac{V_s}{Z_o} = 2.02 \frac{P_{DES}}{V_s}$ $E_{TANK} = 5.36 \frac{P_{DES}}{\omega_o} = 4.45 \frac{P_{DES}}{\omega}$
Short-Circuit Stresses	$V_{cp} = 4.169 V_s$ $I_{LP} = 3.169 \frac{V_s}{Z_o} = 2.52 \frac{P_{DES}}{V_s}$ $E_{TANK} = 10.88 \frac{P_{DES}}{\omega_o} = 9.03 \frac{P_{DES}}{\omega}$ $I_o(sc) = 1.574 I_o(DES)$

The peak current increases by only 25 percent to  $2.52 P_{DES}/V_s$  under short-circuit conditions, with the stored energy doubling to  $9.03 P_{DES}/\omega$ . In contrast, Design A of Table 4.3 (above-resonance) has a full-load tank current of  $2.50 P_{DES}/V_s$ , increasing to  $5.30 P_{DES}/V_s$  under fault conditions. It has much lower tank energy under all conditions, however, about one-fourth of that of Design G at full-load, and one-half under fault conditions.

It was concluded in [27] that above-resonance operation is better, and this is clearly so in terms of the full-load design. However, excellent inherent limiting of the switch and output currents can be obtained from the below-resonance approach, at the expense of about four times the tank-stored energy.

An additional trade-off between above- and below- resonance operation needs to be discussed. The nature of the switching losses is quite different in the two cases. Above-resonance operation requires active interruption of the tank current by the switching devices; however, the switch voltage naturally goes to zero prior to turn-on of the controlled switch. This zero-voltage-switching reduces turn-on losses to zero and permits the use of slow-recovery anti-parallel diodes. Also, the turn-off can be snubbed with lossless snubbers (capacitors) [29]. Below-resonance operation requires that the controlled switches commutate current from their anti-parallel diodes, resulting in switching loss and the need for fast-recovery diodes. Snubbing this commutation requires series inductors and leads to a trapped energy problem. The trapped energy is normally partially recovered and partially dissipated. Turn-off of the controlled switches is automatic, reducing turn-off losses to zero and permitting the use of thyristors.

### SRC Interfacing Capacitors and Transformer

The ratings of the required interface capacitors are now estimated for both above- and below-resonance SRCs. Ripple current in these capacitors can be approximated as that resulting from a full-wave-rectified sinusoid as in [30]. This works best near resonance, due to the low harmonic content of the tank current and the fact that the antiparallel diode conduction angle is small under this circumstance. Away from resonance, the input current  $i_s(t)$  (see Fig. 4.1) will depart from this model due to the increasing angle between tank current zero-crossing and the switching of the controlled bridge. This simple model works better for the output filter capacitor because the uncontrolled-diode bridge switches at current zero-crossings. Also, the tank current is relatively more sinusoidal above-resonance than below, especially when operating away from resonance.

In the case of below-resonance operation, the exact rms tank current is provided by [28]. Knowing that the rms value of  $i_s$  is equal to that of the tank current, the rms ripple current in  $C_s$  can be found from:

$$i_{Cs}(\text{rms}) = \sqrt{i_{TANK}^2(\text{rms}) - I_S^2} \quad . \quad (4.23)$$

The full-load input current  $I_s$  is given by

$$I_s = \frac{P_{DES}}{V_s} \quad , \quad (4.24)$$

where it is understood that  $V_s$  is variable in a variable-frequency design.

Using the design values of  $Z_o$  given by (4.9) together with the entries on Table 4.2 and (4.23 - 4.24), gives input-capacitor ripple currents in the ranges:

$$0.33 \frac{P_{DES}}{V_{s(\min)}} \text{ to } 1.39 \frac{P_{DES}}{V_{s(\min)}} \quad \text{A rms (above resonance)}$$

and

$$0.84 \frac{P_{DES}}{V_{s(\min)}} \text{ to } 1.17 \frac{P_{DES}}{V_{s(\min)}} \quad \text{A rms (below resonance).}$$

The larger values occur at the higher input-side voltages because the dc-input current diminishes while the tank current remains about the same.

The rms ripple current in the output filter capacitor  $C_o$  is found from

$$I_{co}(\text{rms}) = \sqrt{\frac{i_{\text{TANK}}^2(\text{rms})}{N^2} - I_o^2} \quad (4.25)$$

The appropriate output current  $I_o$  can be found on Table 4.1; design values for  $N$  are given by (4.8).

The results of evaluating (4.25) using Tables 4.1 and 4.2 are output-capacitor ripple currents in the ranges:

$$0 \text{ to } 0.98 I_o \quad A \text{ rms (above resonance)}$$

and

$$0.62 I_o \text{ to } 0.55 I_o \quad A \text{ rms (below resonance).}$$

The above-resonance calculations are based on estimated tank rms currents, and thus have uncertain accuracy. As a check, it is noted that a full-wave-rectified-sinusoid model would predict an rms ripple current equal to 48 percent of the corresponding dc current, an rms second-harmonic current equal to 47 percent of the dc current, and high-order harmonics (fourth and up) at 11 percent of dc. The above-resonance case is therefore estimated using the rectified-sinusoid approximation:

$$i_{co}(\text{rms}) = 0.48 I_o.$$

The required values for the input/output capacitors can be estimated on the basis of the rectified-sinusoid model, for which the second-harmonic has a peak value of two-thirds of the dc. For the input capacitor, the predicted ripple factor would be:

$$\begin{aligned} R &= \frac{|v_{s(2)}|}{V_s} = \frac{(\frac{2}{3}I_s)(\frac{1}{2\omega C_s})}{V_s} \\ &= \frac{P_{DES}}{V_s^2} \frac{1}{3\omega C_s} \end{aligned} \quad (4.26)$$



In variable-frequency operation, the worst case of (4.26) occurs at low-line, giving the following design equation for  $C_s$  :

$$C_s = \frac{P_{DES}}{V_s^2(\min)} \frac{1}{3\omega R} \quad (4.27)$$

The switching frequency corresponding to full-load low-line operation is to be used in (4.27).

A design equation for the output capacitor is found using similar considerations.

$$C_o = \frac{P_{DES}}{V_o^2} \frac{1}{3\omega R} \quad (4.28)$$

The minimum switching frequency corresponding to full-load operation is used in (4.28).

The energy stored in  $C_s$  and  $C_o$  is next estimated. For  $C_s$  :

$$E_{CS} = \frac{1}{2} C_s V_s^2 (1 + R_s)^2 = \frac{P_{DES}}{V_s^2(\min)} \frac{V_s^2 (1 + R)^2}{6\omega R}$$

$$E_{CS} = \frac{P_{DES}}{\omega} \frac{K_{TD}^2}{6} \frac{(1 + R)^2}{R} \quad (4.29)$$

The turn-down ratio  $K_{TD}$  in (4.29) is taken to be unity in the case of fixed-input-voltage operation. The switching frequency  $\omega$  is that occurring at  $V_s = V_s(\min)$ .

For  $C_o$ :

$$E_{CO} = \frac{P_{DES}}{\omega} \frac{1}{6} \frac{(1 + R)^2}{R} \quad (4.30)$$

The output-transformer design for below-resonance operation differs somewhat from above-resonance. In the continuous-conduction mode, the transformer exciting voltage is a squarewave at the switching frequency. For above-resonance design, the

controlling case occurs at full-load and low-line. The required volt-second integral is

$$VSI = \frac{1}{n_s} \int_0^{\pi} V_o dt = \frac{\pi V_o}{\omega n_s} \quad \text{volt-sec.} \quad (4.31)$$

(above resonance)

Below-resonance, the worst case occurs at light load with variable-frequency operation, when the frequency reaches one-half the resonant frequency.

The volt-second integral in this case is

$$VSI = \frac{2\pi V_o}{\omega_o n_s} \quad \text{(volt-sec)} \quad (4.32)$$

(below resonance, variable frequency)

Note that (4.32) is given in terms of the resonant frequency  $\omega_o$ . Fixed-frequency below-resonance operation is described by (4.31), where  $\omega$  is the switching frequency. The transformer winding currents are related to the tank currents given previously. For an above-resonance design, the transformer volt-second-ampere product is found using the sinusoidal model for the tank current:

$$VSI \cdot \Sigma ni = \left( \frac{\pi V_o}{\omega_{\min} n_s} \right) \cdot (2n_p i_{TANK(rms)})$$

$$\equiv 6.98 \frac{P_{DES}}{\omega_{\min}} \quad (4.33)$$

where  $\omega_{\min}$  is interpreted as the minimum switching frequency at full-load.

For the below-resonance variable-frequency design recommended on Tables 4.1 and 4.2 the volt-second-ampere product is:

$$\begin{aligned} VSI \cdot \Sigma ni &= \left( \frac{2\pi V_o}{\omega_o n_s} \right) \cdot (2n_p i_{TANK(rms)}) \\ &= \left( \frac{2\pi V_o}{\omega_o} \right) 2.36 I_o \\ &= 14.8 \frac{P_{DES}}{\omega_o} = 12.3 \frac{P_{DES}}{\omega_{\max}} \end{aligned} \quad (4.34)$$

where  $\omega_{\max}$  is interpreted as the maximum switching frequency at full-load ( $\omega_{\max} = 0.83\omega_o$ ).

The previous results for the variable-frequency SRC designs of Tables 4.1 and 4.2 are summarized on Table 4.6. The values for both filter capacitors have been based on second-harmonic currents only along with the switching frequency extreme corresponding to a full-load low-line condition. The rms capacitor currents for the above-resonance case are estimated based on an assumed rms tank current equal to the peak current divided by  $\sqrt{2}$ . The values reported are not considered significantly different than those for the below-resonance case, which were found exactly using the model of [28]. It can be seen that below-resonance operation requires approximately twice the transformer volt-seconds when compared to an above-resonance design having a comparable full-load switching frequency. This is a result of the lowered switching frequency at light loads.

The fixed-frequency SRC designs of Table 4.3 (Design A, above resonance) and Table 4.5 (Design G, below resonance) were also considered. Results pertaining to these are summarized on Table 4.7. It should be noted that the transformer for the below-resonance design can be made substantially smaller due to the fixed-frequency operation.

Table 4.6 Variable-Frequency SRC Interfacing Components

	Above Resonance, Variable Frequency (Refer to Tables 4.1 and 4.2)	Below Resonance Variable Frequency (Refer to Tables 4.1 and 4.2)
Input Filter Capacitor	$C_s = \frac{P_{DES}}{V_s^2(\min)} \frac{1}{3 \omega_{\min} R}$ <p>Ripple Current *:</p> $i_{cs}(\text{rms}) \cong 0.33 \frac{P_{DES}}{V_s(\min)} \text{ to } 1.39 \frac{P_{DES}}{V_s(\min)}$ <p>for <math>V_s = V_s(\min)</math> to <math>2 V_s(\min)</math></p> <p>Stored Energy:</p> $E_{CS} = \frac{P_{DES}}{\omega_{\min}} \frac{K_{TD}^2 (1+R)^2}{6 R}$	$C_s = \frac{P_{DES}}{V_s^2(\min)} \frac{1}{3 \omega_{\max} R}$ <p>Ripple Current:</p> $i_{cs}(\text{rms}) \cong 0.84 \frac{P_{DES}}{V_s(\min)} \text{ to } 1.17 \frac{P_{DES}}{V_s(\min)}$ <p>for <math>V_s = V_s(\min)</math> to <math>2 V_s(\min)</math></p> <p>Stored Energy:</p> $E_{CS} = \frac{P_{DES}}{\omega_{\max}} \frac{K_{TD}^2 (1+R)^2}{6 R}$
Output Filter Capacitor	$C_o = \frac{P_{DES}}{V_o^2} \frac{1}{3 \omega_{\min} R}$ <p>Ripple Current *:</p> $i_{co}(\text{rms}) \cong 0.48 I_o$ <p>Stored Energy:</p> $E_{\omega} = \frac{P_{DES}}{\omega_{\min}} \frac{1}{6} \frac{(1+R)^2}{R}$	$C_o = \frac{P_{DES}}{V_o^2} \frac{1}{3 \omega_{\min} R}$ <p>Ripple Current:</p> $i_{co}(\text{rms}) \cong 0.62 I_o \text{ to } 0.55 I_o$ <p>for <math>V_s = V_s(\min)</math> to <math>2 V_s(\min)</math></p> <p>Stored Energy:</p> $E_{\omega} = \frac{P_{DES}}{\omega_{\max}} \frac{1}{6} \frac{(1+R)^2}{R}$
Output Transformer	<p>Turns Ratio:</p> $N = \frac{n_s}{n_p} = 1.053 \frac{V_o}{V_s(\min)}$ <p>Volt-Second Integral:</p> $VSI = \frac{\pi V_o}{\omega_{\min} n_s}$ <p>Volt-Second-Ampere Product:</p> $VSI \cdot \sum n_i \cong 7.0 \frac{P_{DES}}{\omega_{\min}} = 5.2 \frac{P_{DES}}{\omega_o}$	<p>Turns Ratio:</p> $N = \frac{n_s}{n_p} = 1.111 \frac{V_o}{V_s(\min)}$ <p>Volt-Second Integral:</p> $VSI = \frac{2\pi V_o}{\omega_o n_s}$ <p>Volt-Second-Ampere Product:</p> $VSI \cdot \sum n_i = 12.3 \frac{P_{DES}}{\omega_{\max}} = 14.8 \frac{P_{DES}}{\omega_o}$

\*Estimated based on  $\text{rms} = \text{peak}/\sqrt{2}$   
 $\omega_{\min}$  = minimum full-load frequency  
 $\omega_{\max}$  = maximum full-load frequency

Table 4.7 Fixed-Frequency SRC Interfacing Components

	Above Resonance (Design A, Table 4.3)	Below Resonance (Design G, Table 4.5)
Input Filter Capacitor	$C_s = \frac{P_{DES}}{V_s^2} \frac{1}{3\omega R}$ <p>Ripple Current*:</p> $i_{cs} (rms) \cong 1.46 \frac{P_{DES}}{V_s}$ <p>Stored Energy:</p> $E_{cs} = \frac{P_{DES}}{\omega} \frac{1}{6} \frac{(1+R)^2}{R}$	$C_s = \frac{P_{DES}}{V_s^2} \frac{1}{3\omega R}$ <p>Ripple Current:</p> $i_{cs} (rms) \cong 0.85 \frac{P_{DES}}{V_s}$ <p>Stored Energy:</p> $E_{cs} = \frac{P_{DES}}{\omega} \frac{1}{6} \frac{(1+R)^2}{R}$
Output Filter Capacitor	$C_o = \frac{P_{DES}}{V_o^2} \frac{1}{3\omega R}$ <p>Ripple Current*:</p> $i_{co} (rms) \cong 0.48 I_o$ <p>Stored Energy:</p> $E_{co} = \frac{P_{DES}}{\omega} \frac{1}{6} \frac{(1+R)^2}{R}$	$C_o = \frac{P_{DES}}{V_o^2} \frac{1}{3\omega R}$ <p>Ripple Current:</p> $i_{co} (rms) \cong 0.62 I_o$ <p>Stored Energy:</p> $E_{co} = \frac{P_{DES}}{\omega} \frac{1}{6} \frac{(1+R)^2}{R}$
Output Transformer	<p>Turns Ratio:</p> $N = \frac{n_s}{n_p} = 1.375 \frac{V_o}{V_s}$ <p>Volt-Second Integral:</p> $VSI = \frac{\pi V_o}{\omega n_s}$ <p>Volt-Second-Ampere Product:</p> $VSI \cdot \Sigma ni \cong 7.0 \frac{P_{DES}}{\omega}$	<p>Turns Ratio:</p> $N = \frac{n_s}{n_p} = 1.111 \frac{V_o}{V_s}$ <p>Volt-Second Integral:</p> $VSI = \frac{\pi V_o}{\omega n_s}$ <p>Volt-Second-Ampere Product:</p> $VSI \cdot \Sigma ni \cong 7.4 \frac{P_{DES}}{\omega}$

\*Estimated based on rms = peak/ $\sqrt{2}$

## PARALLEL-LOADED RESONANT INVERTER/CONVERTER

Several variations on the parallel-loaded resonant converter/inverter have appeared in the literature. For use as a dc-dc converter, a variable-frequency topology using a single resonant tank has been analyzed in [31]. Two varieties are considered in [31] - a more conventional form using a current-sourced rectifier on its output-side, and one having distinctly discontinuous conduction of its output rectifier. Both are illustrated in Fig. 4.3. The standard parallel resonant converter (PRC) has a large output inductor  $L_o$  such that the current  $i_o$  can be approximated as low-ripple dc. If  $L_o$  is omitted from Fig. 4.3 while keeping  $C_o$  large enough to maintain low ripple in  $V_o$ , the result is here called the "discontinuous-rectifier-conduction" PRC, or "DRC-PRC." Control of either of these is by means of variation of the switching frequency.

Another technique of control for the PRC is the use of two inverters and phase-shift control [6, 11]. This permits constant-frequency operation. Figs. 4.4 and 4.5 illustrate the application of phase-shift control to a constant-frequency parallel-loaded inverter. If the load contains a current-sourced rectifier, this phase-controlled inverter becomes a dc-dc converter [32]. The circuit of Fig. 4.4 will first be considered as an inverter, the load being assumed to draw an approximately sinusoidal current in response to the low-distortion sinusoidal voltage established by the inverter. This is appropriate for application to an ac distribution system in which low harmonic content is to be maintained. The circuit of Fig. 4.4 will also be considered with a single-phase uncontrolled-rectifier load. This is appropriate to its application as a dc-dc converter, or in an ac system in which no attempt is made to limit harmonic currents.

A constant-frequency PWM-controlled parallel-loaded resonant converter/inverter also appears in the literature [33]. This paper will be briefly reviewed.

### **Variable-Frequency PRC**

The standard PRC is considered first, based on a suggested "good" design of [31]. The basic design information is summarized on Table 4.8, where the input voltage  $V_s$  and output variables  $I_o$  and  $V_o$  are indicated on Fig. 4.3. The design procedure given here assumes load regulation with variable line voltage, and is based on the minimum expected line voltage. The frequency at full load is 60 percent of the resonant frequency, and increases through the resonant frequency at high line, light load or under short-circuit conditions.

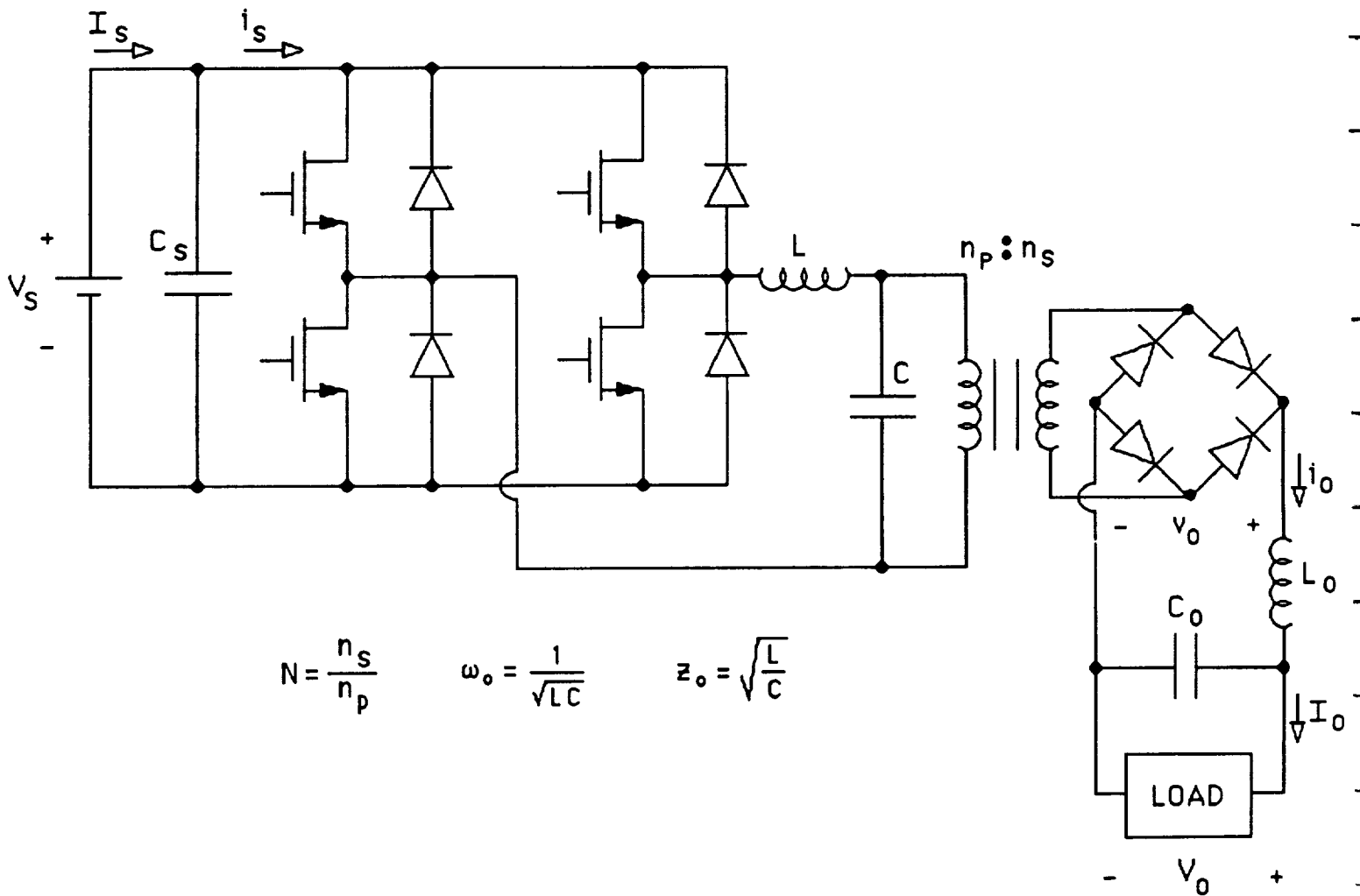


Fig. 4.3 Parallel-loaded resonant converter. The standard PRC has a large  $L_o$  such that  $i_o$  has low ripple. The discontinuous-rectifier- conduction PRC omits  $L_o$ .



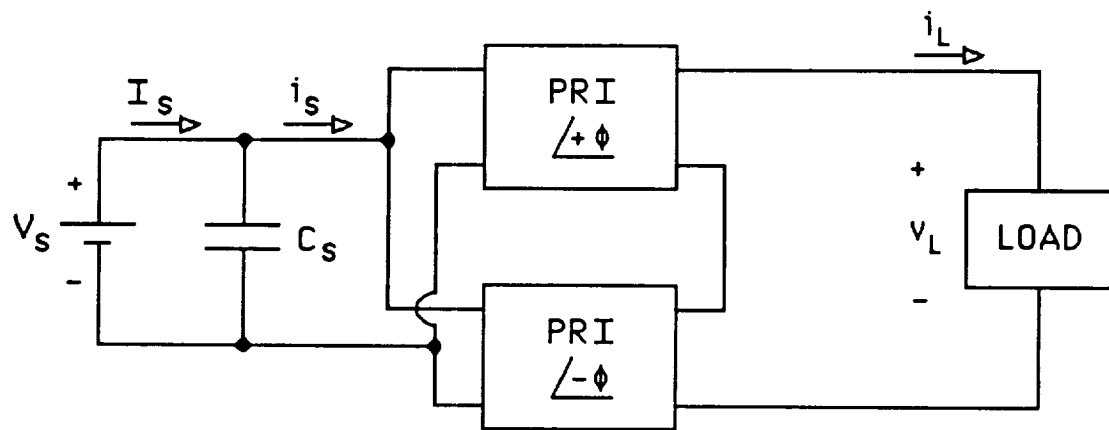


Fig. 4.4 Phase-controlled parallel-resonant inverter. A typical unit inverter is shown in Fig. 4.5.

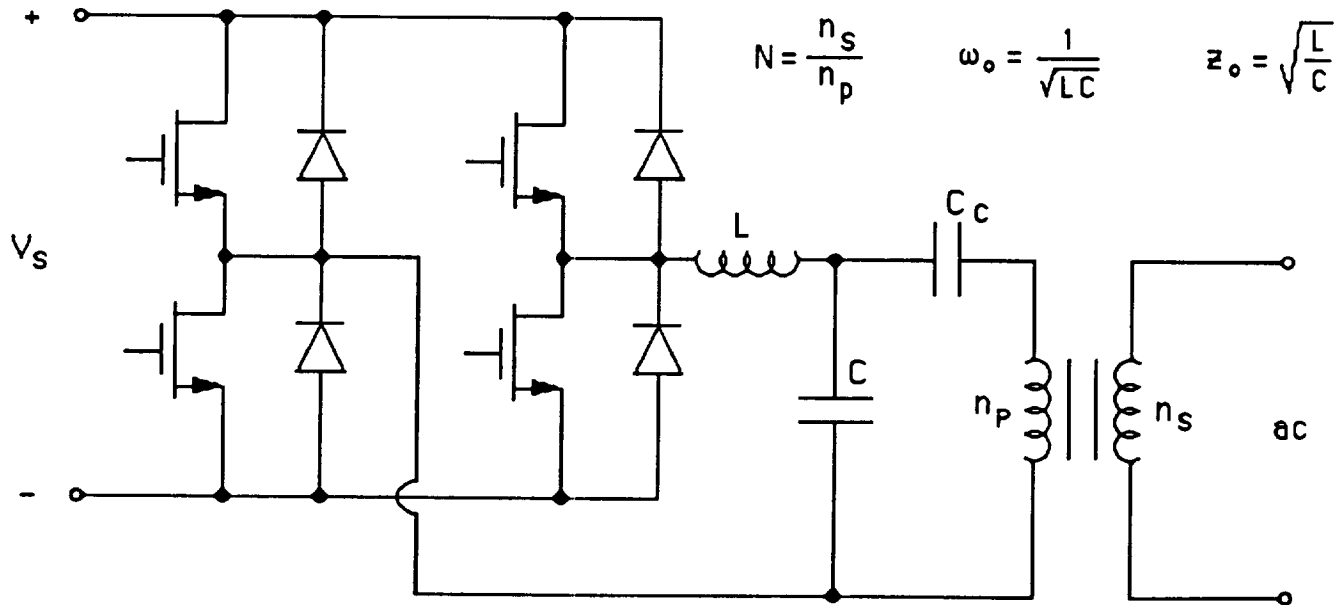


Fig. 4.5 Typical unit inverter used in Fig. 4.4.

Another possibility is a design based on above-resonance operation under all conditions, including load short-circuit. It appears that similar circuit stresses will occur for this design, although further study would be required to quantify this. A completely below-resonance design is not possible if load short-circuit is to be considered. Table 4.8 also presents an unusual design suggested in [31] which omits the inductor  $L_o$  of Fig. 4.3. This DRC-PRC design has a similar peak tank current but a lower tank voltage when compared with the standard. Table 4.8 includes estimates of peak tank voltage and current at high line ( $V_s = 2V_s(\min)$ ); these were taken from graphs found in [31].

The interface component ratings for Design A of Table 4.8, the standard PRC, are now estimated. The input filter capacitor is found using the same considerations as those of (4.23) - (4.27). The tank rms current is approximated as being equal to the peak value divided by  $\sqrt{2}$ . The estimated ripple current in Table 4.9 is given for  $V_s = 2V_s(\min)$ . The output filter inductor is assumed to support the ripple components of the full-wave-rectified voltage given by  $v_o(t) = NV_{CP}\sin \omega t$ . The inductor supports the difference between  $v_o$  and its average value  $V_o = (2NV_{CP})/\pi$ . The expected peak-to-peak ripple current is therefore:

$$i_o(p-p) = \frac{1}{\omega L_o} \int_{\alpha}^{\pi-\alpha} NV_{CP} \left( \sin \omega t - \frac{2}{\pi} \right) d\omega t \quad (4.35)$$

where  $NV_{CP}\sin \alpha = \frac{2}{\pi} NV_{CP}$ .

Table 4.8 Variable-Frequency PRC Designs

	Design A Current-Sourced Rectifier	Design B Discontinuous-Rectifier Conduction
Output Voltage	$V_o = 1.05 N V_{s(\min)}$	$V_o = 1.21 N V_{s(\min)}$
Output Current	$I_o = 1.55 \frac{V_{s(\min)}}{N Z_o}$	$I_o = 1.20 \frac{V_{s(\min)}}{N Z_o}$
Turns Ratio	$N = 0.952 \frac{V_o}{V_{s(\min)}}$	$N = 0.826 \frac{V_o}{V_{s(\min)}}$
Characteristic Impedance	$Z_o = 1.63 \frac{V_s^2(\min)}{P_{DES}}$	$Z_o = 1.45 \frac{V_s^2(\min)}{P_{DES}}$
Peak Tank Current	$I_{LP} = 1.56 \frac{P_{DES}}{V_{s(\min)}} \quad *$ $(I_{LP} \cong 2.1 \frac{P_{DES}}{V_{s(\min)}}) \quad +$	$I_{LP} = 1.52 \frac{P_{DES}}{V_{s(\min)}} \quad *$ $(I_{LP} \cong 2.4 \frac{P_{DES}}{V_{s(\min)}}) \quad +$
Peak Tank Voltage	$V_{cp} = 2.00 V_{s(\min)} \quad *$ $(V_{cp} \cong 2 V_{s(\min)}) \quad +$	$V_{cp} = 1.21 V_{s(\min)} \quad *$ $(V_{cp} \cong 1.2 V_{s(\min)}) \quad +$
Full-Load Frequency	$\omega \geq 0.6 \omega_o \quad *$	$\omega \geq 0.6 \omega_o \quad *$
Tank Energy	$E_{TANK} \cong 4.8 \frac{P_{DES}}{\omega_o} = 2.9 \frac{P_{DES}}{\omega_{\min}}$	$E_{TANK} \cong 2.2 \frac{P_{DES}}{\omega_o} = 1.3 \frac{P_{DES}}{\omega_{\min}}$

\*Evaluated at  $V_s = V_{s(\min)}$

+Estimated from graph at  $V_s = 2V_{s(\min)}$

The ripple factor for the inductor current is defined as one-half the peak-to-peak current divided by the average current. The ripple factor is therefore:

$$R = \frac{i_o(p-p)}{2I_o} = \frac{NV_{cp}}{2\omega L_o I_o} \left[ -\cos \omega t - \frac{2}{\pi} \omega t \right]_{\alpha}^{\pi-\alpha}$$

$$= 0.641 \frac{V_o}{\omega L_o I_o} \quad \text{where}$$

$$V_o \cong \frac{2}{\pi} NV_{cp} \text{ and } \alpha = \sin^{-1} \frac{2}{\pi} . \quad (4.36)$$

Equation (4.36) provides a means for sizing  $L_o$  to obtain a given ripple factor. The peak stored energy in  $L_o$  is therefore:

$$E_{LO} = \frac{1}{2} L_o I_o^2 (1 + R)^2 = \frac{P_{DES}}{\omega_{min}} 0.320 \frac{(1 + R)^2}{R} . \quad (4.37)$$

The transformer volt-second-integral for the standard PRC is estimated based on a sinusoidal voltage waveform:

$$VSI = \frac{1}{n_s \omega} \int_0^{\pi} \left( \frac{\pi V_o}{2} \right) \sin \omega t \, d\omega t = \frac{\pi V_o}{n_s \omega_{min}} . \quad (4.38)$$

The volt-second-ampere product is therefore:

$$VSI \cdot \Sigma ni = \left( \frac{\pi V_o}{n_s \omega_{min}} \right) [2I_o n_s] = \frac{P_{DES}}{\omega_{min}} 2\pi . \quad (4.39)$$

The results of (4.35) - (4.39) are entered on Table 4.9 for Design A, a standard PRC.

The DRC-PRC of Table 4.8 (Design B) is next considered. The input capacitor is sized using the same considerations as those of Design A; therefore, the results of (4.23) - (4.27) are also used here.

Inspection of the sample waveforms of [31] reveals that the output current ( $i_o$ ) in this PRC is approximately triangular in shape, having an average value of  $I_o$ . For such a waveform, the following relations apply:

$$\begin{aligned} i_o(\text{peak}) &= 2I_o \text{ and} \\ i_o(\text{rms}) &= \frac{2}{\sqrt{3}}I_o. \end{aligned} \quad (4.40)$$

The rms ripple current in  $C_o$  is estimated on the basis of (4.40).

$$i_{co}(\text{rms}) \cong \sqrt{\left(\frac{2I_o}{\sqrt{3}}\right)^2 - I_o^2} = 0.882 I_o \quad (4.41)$$

The ripple factor is given by

$$R = \frac{v_o(\text{peak})}{V_o} = \frac{\tau I_o}{2C_o V_o} \quad (4.42)$$

where  $\tau$  is the time duration of the triangular current pulse. Because  $\tau$  cannot exceed half the switching period, a pessimistic estimate for  $C_o$  is given by:

$$C_o = \frac{P_{DES}}{V_o^2} \frac{1}{4fR}. \quad (4.43)$$

The peak stored energy in  $C_o$  is therefore:

$$E_{CO} = \frac{1}{2}C_o V_o^2(1 + R)^2 = \frac{P_{DES}}{\omega_{\min}} \frac{2\pi(1 + R)^2}{8R}. \quad (4.44)$$

The transformer volt-second integral is conservatively estimated based on a square-wave voltage (the actual waveform is trapezoidal):

$$VSI \leq \frac{V_o}{2fn_s}. \quad (4.45)$$

The volt-second-ampere product is found using (4.40):

$$VSI \cdot \Sigma n_i = \frac{P_{DES}}{\omega_{min}} \frac{4\pi}{\sqrt{3}} \quad (4.46)$$

These results are also entered on Table 4.9.

Table 4.9 Interface Components for the Variable-Frequency  
PRC Designs of Table 4.8

	Design A Current-Sourced Rectifier	Design B Discontinuous-Rectifier Conduction
Input Filter Capacitor	$C_s = \frac{P_{DES}}{V_s^2(\min)} \frac{1}{3\omega_{\min}R}$ <p>Ripple Current*:</p> $i_{cs}(\text{rms}) \cong 1.4 \frac{P_{DES}}{V_s(\min)}$ <p>Stored Energy:</p> $E_{cs} = \frac{P_{DES}}{\omega_{\min}} \frac{K_{TD}^2}{6} \frac{(1+R)^2}{R}$	$C_s = \frac{P_{DES}}{V_s^2(\min)} \frac{1}{3\omega_{\min}R}$ <p>Ripple Current*:</p> $i_{cs}(\text{rms}) \cong 1.6 \frac{P_{DES}}{V_s(\min)}$ <p>Stored Energy:</p> $E_{cs} = \frac{P_{DES}}{\omega_{\min}} \frac{K_{TD}^2}{6} \frac{(1+R)^2}{R}$
Output Filter	$L_o = \frac{P_{DES}}{I_o^2} \frac{0.641}{R \omega_{\min}}$ <p>Stored Energy:</p> $E_{LO} = \frac{P_{DES}}{\omega_{\min}} 0.320 \frac{(1+R)^2}{R}$	$C_o = \frac{P_{DES}}{V_o^2} \frac{1}{4fR}$ <p>Stored Energy:</p> $E_{co} = \frac{P_{DES}}{\omega_{\min}} \frac{\pi}{4} \frac{(1+R)^2}{R}$
Output Transformer	<p>Turns Ratio:</p> $N = \frac{n_s}{n_p} = 0.952 \frac{V_o}{V_s(\min)}$ <p>Volt-Second Integral:</p> $VSI = \frac{\pi V_o}{\omega n_s}$ <p>Volt-Second-Ampere Product:</p> $VSI \cdot \Sigma ni = 2\pi \frac{P_{DES}}{\omega_{\min}}$	<p>Turns Ratio:</p> $N = \frac{n_s}{n_p} = 0.826 \frac{V_o}{V_s(\min)}$ <p>Volt-Second Integral:</p> $VSI \leq \frac{V_o}{2fn_s}$ <p>Volt-Second-Ampere Product:</p> $VSI \cdot \Sigma ni = \frac{P_{DES}}{\omega_{\min}} \frac{4\pi}{\sqrt{3}}$

\*Estimate based on  $\text{rms} = \text{peak}/\sqrt{2}$ ;  $V_s = 2V_s(\min)$   
 $\omega_{\min}$  = minimum full-load switching frequency

### **Phase-Controlled PRI**

The phase-controlled parallel-loaded resonant inverter (PC-PRI) is shown in Figs. 4.4 and 4.5. The intent of this topology is the production of a low-distortion sinusoidal voltage on the load, which may actually be an ac distribution bus. Two individual inverters are used, each of which operates at fixed frequency but variable relative phase. The output "compensating" capacitor can be chosen to reduce the fundamental-frequency output reactance to zero. The load is initially assumed to draw a sinusoidal current; it is therefore not a simple rectifier, but perhaps a high-power-factor rectifier, or of a resistive nature, such as heating and lighting. The steady-state analysis and design procedure for Fig. 4.4 is taken from [11] and [34].

An implementation of the PC-PRI based on the Mapham inverter is also possible [7]. This circuit performs similarly to Fig. 4.4 in most respects. It is particularly appropriate for use with SCRs as discussed in [35], but it does expose the switches to multiplied blocking voltages. The Mapham-inverter-based PC-PRI is not discussed further because recent advances in the available switching devices tend to rule out the use of SCRs.

Two suggested designs, Design C for below-resonance operation, and Design D for above-resonance operation, are taken from [11] and summarized on Table 4.10. It is found [11] that a compromise between output waveform distortion and tank component energy storage must be made in choosing the switching/resonant frequency ratio. The ratios 0.65 and 1.5 are used here for below- and above-resonance operation, respectively.

The switching device ratings are independent of this choice, however, being only a function of the design full-load volt-ampere rating of the inverter ( $S_{DES}$ ). The suggested design procedure provides (ideally) zero output impedance and perfect load regulation. The load current must be limited by a current feedback loop which can



reduce the output voltage to essentially zero. The transformer turns-ratio is set to provide the desired rms output voltage at minimum input voltage. From [11]:

$$v_L(\text{rms}) = N \frac{8V_s \cos \phi}{\sqrt{2}\pi \left| 1 - \left( \frac{\omega}{\omega_o} \right)^2 \right|}, \quad 0 \leq \phi \leq \frac{\pi}{2}. \quad (4.47)$$

Therefore

$$N = 0.321 \frac{v_L(\text{rms})}{V_s(\text{min})} \quad (\text{below resonance})$$

and

$$N = 0.694 \frac{v_L(\text{rms})}{V_s(\text{min})} \quad (\text{above resonance}) \quad (4.48)$$

The tank impedance is chosen such that reversal of the expected commutation sequence of the switching devices cannot occur at or below rated load current. This produces the design equation:

$$Z_o \leq \frac{4V_s(\text{min})}{\sqrt{2}\pi N i_L(\text{rms})} \frac{\omega}{\omega_o} \quad (4.49)$$

Therefore

$$Z_o = \sqrt{\frac{L}{C}} = 1.825 \frac{V_s^2(\text{min})}{S_{DES}} \quad (\text{below resonance})$$

and

$$Z_o = 1.945 \frac{V_s^2(\text{min})}{S_{DES}} \quad (\text{above resonance}). \quad (4.50)$$

For a given switching frequency and switching/resonant frequency ratio,  $\omega_o$  is readily chosen, and  $Z_o$  is given by (4.50). The tank elements are then determined:

$$L = \frac{Z_o}{\omega_o} \text{ and } C = \frac{1}{\omega_o Z_o}. \quad (4.51)$$

The compensating capacitor  $C_c$  in Fig. 4.5 is chosen to null the output impedance; thus  $C_c = 1.367C$  for below-resonance operation. Above-resonance operation requires a compensating inductor  $L_c = 0.800L$  in place of  $C_c$ . These results are summarized on Table 4.10. Expressions for peak tank inductor current, peak tank capacitor voltage and peak compensating reactor voltage/current are also given on Table 4.10. Note that these are given as functions of the design turn-down ratio  $K_{TD} \equiv V_s(\text{max})/V_s(\text{min})$ . It should also be noted that these are worst-case ratings, and do not all occur simultaneously.

Table 4.10 also gives a total stored energy which is the sum of the peak stored energy ratings of all six tank and compensating reactances. This total was calculated for a design turn-down ratio of 2. It can be noted that a below-resonance design generally requires much smaller tank components than an above-resonance design.

The second-harmonic ripple current appearing on the input side of the inverter is next estimated based on [11]. The contributions of the two unit inverters are found to be directly additive for a control angle  $\phi = 0$ , which corresponds to  $V_s = V_s(\text{min})$ . This ripple current is greatest in the somewhat unlikely case of a purely inductive load, or 70 percent as much for a unity-power-factor load. The estimated second-harmonic ripple current is:

$$i_{s(2)} = \frac{32}{\pi^2} \left| \frac{\left(\frac{\omega}{\omega_0}\right)}{1 - \left(\frac{\omega}{\omega_0}\right)^2} \right| \frac{V_s(\text{min})}{Z_o} \quad \text{A peak} \quad (4.52)$$

for  $\phi = 0$  and design full-load, inductive.

Whether above or below resonance, (4.52) produces an estimate of the second-harmonic ripple current of

$$|i_{s(2)}| = 2 \frac{S_{DES}}{V_s(\text{min})} \quad \text{A peak.} \quad (4.53)$$

The rms ripple current in the input capacitor can be estimated under the assumption that all ripple components of both unit inverters are directly additive. This occurs when the control angle  $\phi = 0$  and  $V_s = V_s(\min)$ . If the loading is purely reactive, then the input ripple is equal to twice the rms value of either tank current. Using the value given on Table 4.10 for  $K_{TD} = 1$ :

$$i_{SC}(\text{rms}) = 2.22 \frac{S_{DES}}{V_s(\min)} \quad (\text{reactive load}) \quad . \quad (4.54)$$

With a resistive load, this would reduce to:

$$i_{SC}(\text{rms}) = 1.99 \frac{S_{DES}}{V_s(\min)} \quad (\text{resistive load}) \quad . \quad (4.55)$$

The input voltage ripple factor can be estimated on the basis of the second-harmonic component by using (4.53), giving:

$$R = \frac{S_{DES}}{V_s^2(\min)} \frac{1}{\omega C_s} \quad (4.56)$$

The peak stored energy in  $C_s$  at high line then becomes:

$$E_{CS} = \frac{S_{DES}}{\omega} \frac{K_{TD}^2}{2} \frac{(1 + R)^2}{R} \quad (4.57)$$

The output transformer of Fig. 4.5 processes the output volt-amperes of one of the two unit inverters. Because of the phase-shift control, these individual transformer voltages each differ in phase from the output voltage  $v_L$  by  $\phi$ , the control angle. The control angle is related to the input voltage by:

$$\cos \phi = \frac{V_s(\min)}{V_s} \quad (4.58)$$

Therefore, the required volt-ampere rating of either transformer is

$$S_{\text{TRANS}} = \frac{1}{2} \frac{S_{\text{DES}}}{\cos \phi} = \frac{1}{2} S_{\text{DES}} K_{\text{TD}} . \quad (4.59)$$

Because the transformer waveforms are assumed sinusoidal, the total volt-second integral and volt-second-ampere product are readily found:

$$V_{\text{SI}} = \frac{2\sqrt{2} v_{\text{L}}(\text{rms})}{\omega n_s} K_{\text{TD}} \quad \text{and} \quad (4.60)$$

$$V_{\text{SI}} \cdot \Sigma n_i = \frac{S_{\text{DES}}}{\omega} 4\sqrt{2} K_{\text{TD}} . \quad (4.61)$$

The above expressions represent the total ratings of both transformers. The results of (4.52) - (4.61) are summarized on Table 4.11.

Table 4.10 Suggested PC-PRI Design

	Design C Below-Resonance	Design D Above-Resonance
Resonant Frequency	$\omega_o = \frac{\omega}{0.65}$	$\omega_o = \frac{\omega}{1.5}$
Transformer Turns-Ratio	$N = \frac{n_s}{n_p} = 0.321 \frac{V_L(\text{rms})}{V_s(\text{min})}$	$N = \frac{n_s}{n_p} = 0.694 \frac{V_L(\text{rms})}{V_s(\text{min})}$
Tank Impedance	$Z_o = 1.825 \frac{V_s^2(\text{min})}{S_{DES}}$	$Z_o = 1.945 \frac{V_s^2(\text{min})}{S_{DES}}$
Compensating Reactor	$C_c = 1.367 C$	$L_c = 0.800 L$
Peak Tank Current	$I_{LP} = 0.786 (1 + K_{TD}) \frac{S_{DES}}{V_s(\text{min})}$	$I_{LP} = 0.786 (1 + K_{TD}) \frac{S_{DES}}{V_s(\text{min})}$
Peak Tank Voltage	$V_{CP} = 2.205 (0.422 + K_{TD}) V_s(\text{min})$	$V_{CP} = 1.019 (2.25 + K_{TD}) V_s(\text{min})$
Peak Compensating Voltage/Current	$V_{CCP} = 0.932 V_s(\text{min})$	$I_{LCP} = 0.982 \frac{S_{DES}}{V_s(\text{min})}$
Peak Stored Energy Rating	$E_{TOTAL} = 17.2 \frac{S_{DES}}{\omega} \cdot$	$E_{TOTAL} = 32.9 \frac{S_{DES}}{\omega} \cdot$
Total Conduction Loss, Four Devices +	$\frac{P_{COND}}{S_{DES}} = 2.47 (1 + K_{TD}^2) K_{TD} \left( \frac{S_{DES}}{V_s(\text{min})} \right) K V_s^{1.5}(\text{max})$	

\*Total of six component ratings, evaluated for  $K_{TD} = 2$

+At high line, unity pf load

Table 4.11 Interface Components for the  
PC-PRI Designs of Table 4.10

	Design C Below-Resonance	Design D Above-Resonance
Input Filter Capacitor	$C_s = \frac{S_{DES}}{V_s^2(\min)} \frac{1}{\omega R}$ <p>Ripple Current:</p> $i_{cs}(\text{rms}) = 2.2 \frac{S_{DES}}{V_s(\min)}$ <p>(reactive load)</p> <p>Stored Energy:</p> $E_{cs} = \frac{S_{DES}}{\omega} \frac{K_{TD}^2}{2} \frac{(1 + R)^2}{R}$	$C_s = \frac{S_{DES}}{V_s^2(\min)} \frac{1}{\omega R}$ $i_{cs}(\text{rms}) = 2.2 \frac{S_{DES}}{V_s(\min)}$ <p>(reactive load)</p> $E_{cs} = \frac{S_{DES}}{\omega} \frac{K_{TD}^2}{2} \frac{(1 + R)^2}{R}$
Output Transformer (Each)	<p>Turns Ratio:</p> $N = \frac{n_s}{n_p} = 0.321 \frac{v_L(\text{rms})}{V_s(\min)}$ <p>Volt-Second Integral:</p> $VSI = \frac{\sqrt{2} K_{TD} v_L(\text{rms})}{\omega n_s}$ <p>Volt-Second-Ampere Product:</p> $VSI \cdot \Sigma ni = \frac{S_{DES}}{\omega} 2\sqrt{2} K_{TD}$	$N = 0.694 \frac{v_L(\text{rms})}{V_s(\min)}$ <p>Volt-Second Integral:</p> $VSI = \frac{\sqrt{2} K_{TD} v_L(\text{rms})}{\omega n_s}$ <p>Volt-Second-Ampere Product:</p> $VSI \cdot \Sigma ni = \frac{S_{DES}}{\omega} 2\sqrt{2} K_{TD}$

### **PC-PRI with Rectifier Load**

The use of a single-phase phase-controlled rectifier with the PC-PRI has been investigated [32]. In this reference, the ac-side load current was modeled as a square wave with variable phase relative to the ac-side voltage. Compensating reactors were not included. It was found that a highly-distorted ac-side waveform could result under heavy loading, which for the authors of [32] defined an upper boundary on the load current. Although a detailed analysis of the critical value of the load current was not given, a spot check of the data given in [32] implies that the critical current is probably somewhat above the limit given by [11], considering only the fundamental-frequency component of this current.

In any case, the heavy use of standard single-phase rectifiers on an ac distribution system raises some unanswered questions. No studies seem to have been made of the impact these rectifier-generated harmonic currents would have on the operation of the transmission lines or other loads on the system. If the rectifier load is limited to a suitable level, reasonably sinusoidal voltage could be maintained at the inverter output; however, the harmonic currents will cause voltage drops on the transmission-line series impedances, and may excite resonance involving power-factor-correcting capacitors, if present. Because most references emphasize the low-distortion waveforms possible with the PC-PRI, it seems that the majority of the load rectifiers used in this system will need either passive harmonic traps or active harmonic-reduction techniques.

The reduced-harmonic rectifiers needed for the dc loads on the PC-PRI constitute a weight, cost and loss to be charged against this system in the same manner as additional dc-dc converters needed by various loads must be charged against a dc transmission system. The PC-PRI is not considered practical for use with standard single-phase rectifiers, and therefore is not considered further.

### **Pulse-Width-Controlled PRI**

An alternate means of obtaining constant frequency operation of the PRI is discussed in [33], in which it is called "clamped-mode." However, the means of regulation proposed in [33] is essentially pulse-width-modulation of the switch matrix which drives the single parallel-loaded resonant tank, and thus will be referred to here as PWM control, or PWM-PRI. A sample waveform is shown in Fig. 4.6. A full-bridge inverter (not shown) drives the resonant tank of Fig. 4.6 with the pulse-width-modulated waveform  $v(t)$ . Reduction of the pulse width of  $v(t)$  reduces its fundamental-frequency content, and thus provides a means of line regulation. The series capacitor  $C_c$  can be chosen to give good load regulation as with the PC-PRI.

Operation with all switching devices receiving zero-current turn-off is possible [33], but only over restricted control and load ranges. Conduction currents and losses are not the same for all switching devices. To maintain this natural commutation, a fairly high tank current relative to the load current is needed [33]. Therefore, operation with two of the switching devices interrupting current is proposed.

This type of design would require dissimilar snubbers for the two bridge switching legs in a high-power application. Also, the mode boundaries would have to be honored to avoid reversal of the expected commutation sequences of any diode-transistor pair. Operation at a switching frequency of  $1.35\omega_0$ , where  $\omega_0$  is the natural resonant frequency, seems to be suggested in [33]. However, there is no other clear design procedure suggested.



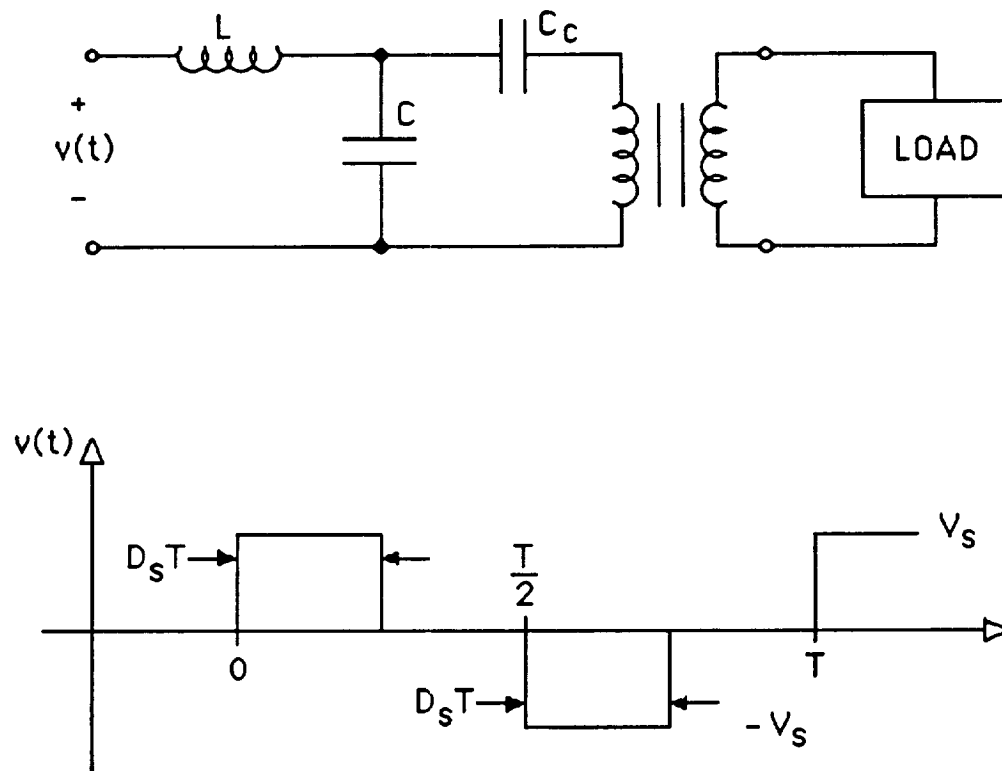


Fig. 4.6 Sample PWM-PRF waveform. (The bridge inverter generating  $v(t)$  from a dc source of  $V_s$  is not shown.)

### TRW Resonant Inverter

The TRW resonant inverter [15, 18, 36] appears to be a resonant adaptation of the TRW converter discussed in a previous chapter. That converter consisted of a buck converter providing the current source for a current-fed transformer. As pointed out previously, operation of the buck converter with near to its critical inductance could reduce the switching losses substantially in the current-fed-transformer switching devices. However, the buck converter itself still must suffer switching losses, especially at turn-off. Similarly, the resonant inverter has a current-fed transformer, except that the dc-side inductor is resonated with an ac-side capacitor, which is parallel loaded. The switching losses in the transformer switching devices are zero at light load, due to zero-current turn-on and turn-off. The buck converter switch must still turn-off near the peak resonant current. At heavy loads or load short-circuit, there are switching losses in all switches. The output voltage is a low distortion sinusoid. The circuit of [15, 18, 36] is shown in Fig. 4.7.

Although only limited details of the intended design and operation procedures are available, the equivalent circuits of Fig. 4.8 can be deduced from [15]. This figure applies to "clocked-mode" operation below rated load. (Clocked-mode operation means that the switching frequency is fixed, each column of Fig. 4.8 taking one-half of the switching period.) Referring to the left-hand column of Fig. 4.8, there is first a "PWM interval" during which energy is taken from the dc source. The duration of this interval is a control input. Next is a "free-wheeling interval" during which there is damped resonance of L, C and load. Finally, there is a brief "zero-current interval" which occurs at light load.

This zero-current interval disappears at heavy load (or load short-circuit) due to the lowering of the LC ringing frequency by load damping.

The right-hand column of Fig. 4.8 is symmetric to the left, and represents the second half-cycle of the switching frequency.

The simulation waveforms of [15] indicate that even under normal steady-state conditions, the PWM switch (Q3 or Q3') must interrupt nearly the peak resonant current to cause the transition from the PWM interval to the free-wheeling interval. Therefore, it does not seem that this approach yields any benefits in terms of switching losses.

Indeed, the steady-state switching losses in Q3 and Q3' would seem to be much greater than those of a well-designed buck converter of equal power. The transformer-fed switches (Q1 and Q2) normally do receive zero-current switching, but this benefit is lost under load-fault conditions, and therefore cannot be relied on in the design of their snubbers. This inverter does apparently offer a well-filtered sinusoidal output.

The equivalent circuits of Fig. 4.8 suggest an alternate push-pull implementation of the TRW resonant inverter. This is shown in Fig. 4.9. Transistors Q1 and Q2 are driven with a 50 percent duty cycle, as in Fig. 4.7. Transistor Q3 is pulse-width-modulated, and performs the function of both Q3 and Q3' of Fig. 4.7.

This alternate implementation also has the equivalent circuits of Fig. 4.8, but does eliminate a switching device (Q3'), and also makes the functions of the various parts more evident. It can be seen in Fig. 4.9 that this resonant inverter is essentially a buck converter feeding a parallel-loaded resonant inverter. The pulsating nature of the inductor current precludes a separate analytical treatment of the buck converter and resonant inverter portions of the circuit, however. A full-bridge equivalent to Fig. 4.9 is readily apparent. A half-bridge equivalent is also possible, although not particularly practical due to the use of two feed inductors.

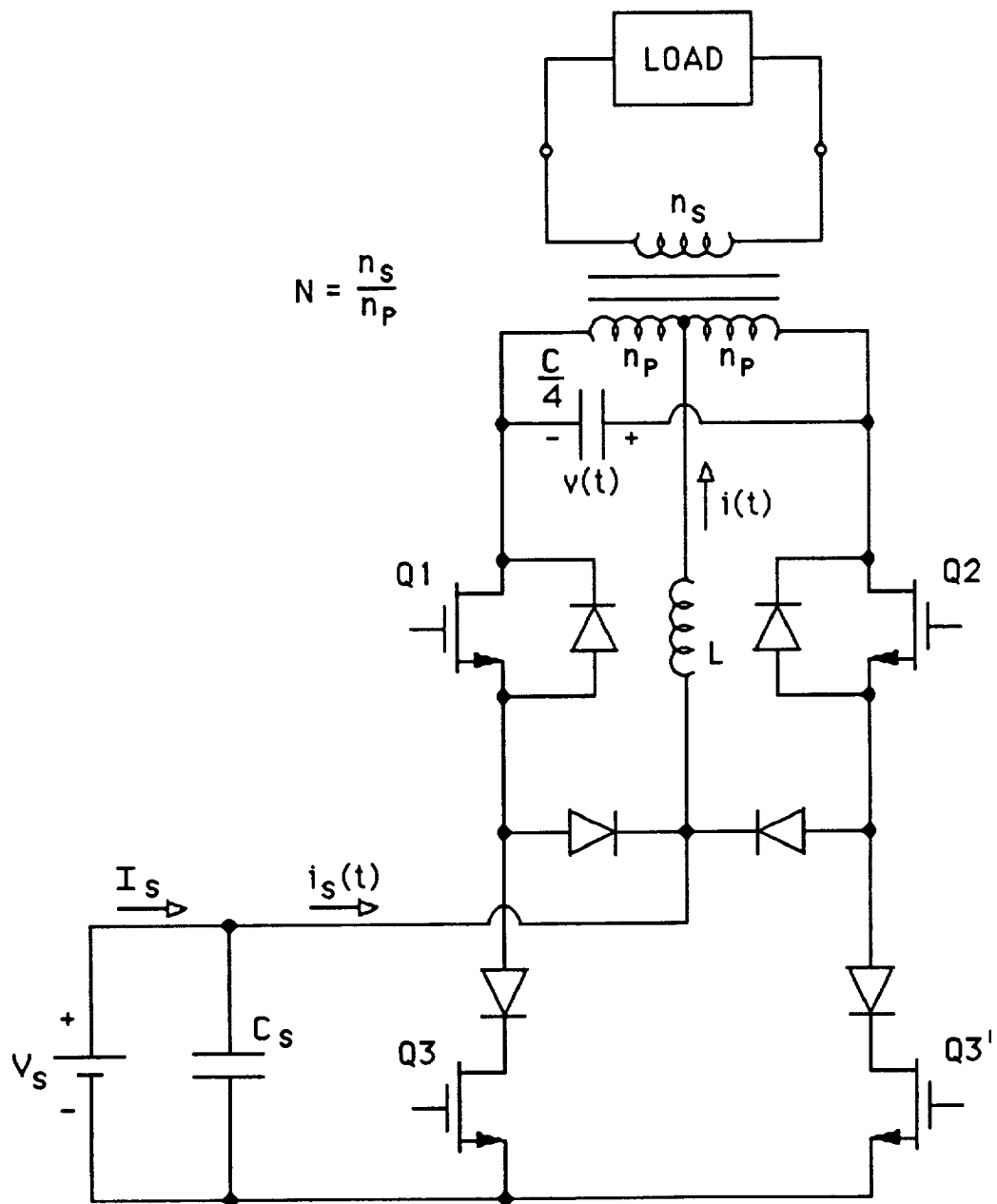
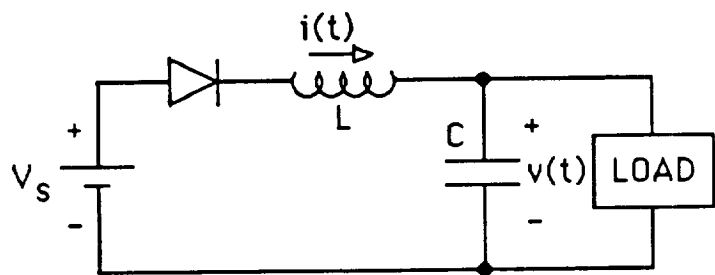
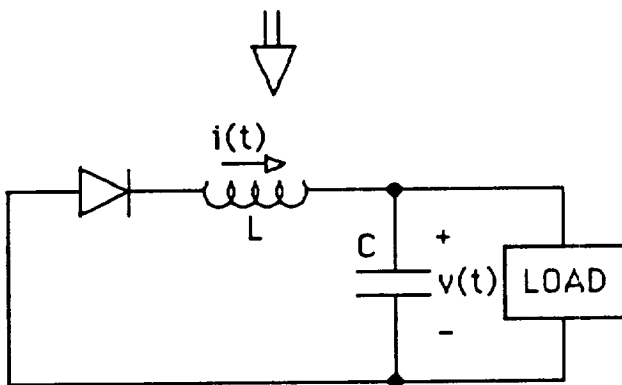
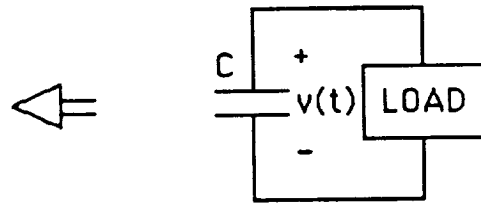


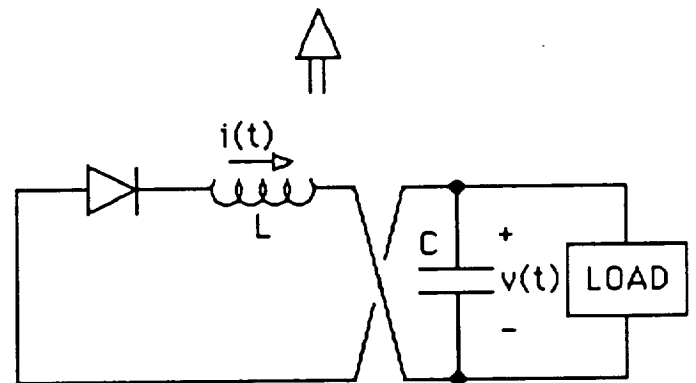
Fig. 4.7 TRW resonant inverter.



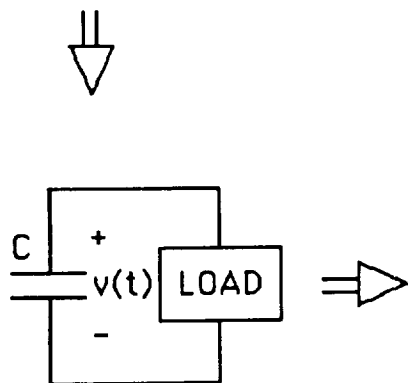
Q1, Q3 ON PWM Interval



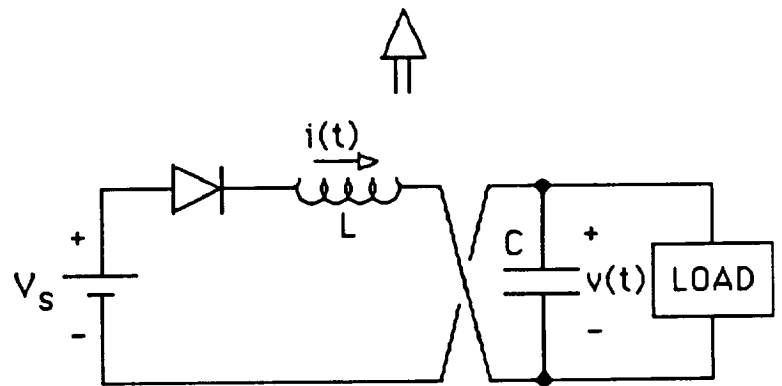
Q1 ON Free-Wheeling Interval



Q2 ON



Zero-Current Interval



Q2, Q3' ON

Fig. 4.8 Equivalent circuits for the TRW resonant inverter (transformer turns ratio taken to be unity).

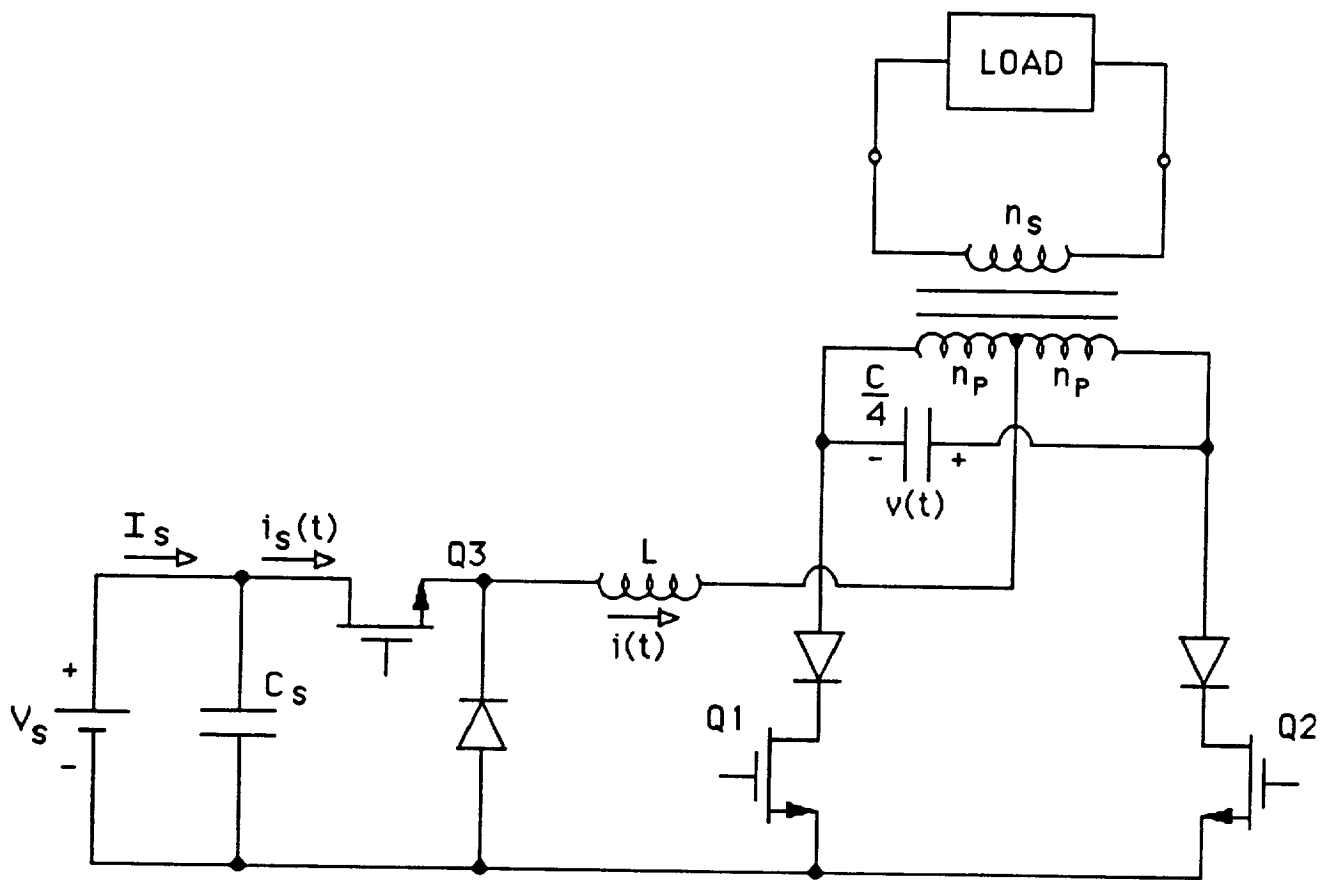


Fig. 4.9 Alternate implementation of the TRW resonant inverter.

## V COMPARATIVE STUDIES

### DC-DC CONVERTERS

The purpose of this section is the comparative study of the dc-dc converters discussed previously. If a dc transmission and distribution system is selected, the source dc-dc converter will be at the heart of it. The topologies reviewed here are ranked according to their suitability to this purpose.

Five dc-dc converters are compared based on the following assumptions: a source-voltage turn-down ratio  $K_{TD} = 2$ , 5 percent ripple on voltage-interfacing capacitors and 10 percent ripple on current-interfacing inductors (at full-load current levels). Four identical ohmic switching devices are assumed for each converter; they are assumed to follow the model  $R_{DS} = K V^{2.5}$ .

Table 5.1 compares the five dc-dc converters in terms of conduction loss, transformer size, energy stored in the interface components and resonant-tank-stored energy. The buck converter is readily seen to have the lowest conduction losses and stored energy of the alternatives. The major negative factor is the switching losses, which include both turn-on and turn-off components. A secondary factor would be the transformer leakage flux (neglected in this comparison), which increases the effective turn-down ratio requirement of the design.

The above-resonance SRC is a very attractive resonant alternative. Multiplied conduction loss is the price paid for elimination of the turn-on switching losses. This topology is also eligible for lossless snubbers, so turn-off losses can be greatly reduced. The above-resonance SRC is particularly favorable due to its modest tank-stored energy, relative to the other resonant converters.

The below-resonance SRC is an alternative when zero-current switch turn-off is desired. There are two disadvantages: the larger transformer required and the substantially larger resonant tank. This topology is well proven for use with thyristors at high power levels.

The parallel-loaded resonant converters are also useful alternatives to the SRC, particularly if a high turns-ratio transformer is required. In this case, both the transformer leakage inductance and secondary distributed capacitance can be incorporated into the resonant tank. If the resonant capacitor can be moved to a higher-voltage transformer secondary, better dielectric utilization can be obtained.

One practical issue in the design of the PRC not considered here is that of a dc block for the transformer primary. The addition of a series capacitor is simple, but costly due to its high current and stored energy. A duty-cycle-balancing mechanism in the controller would seem preferable at high power levels.

The DRC-PRC shows a substantially higher interface-stored energy primarily due to the large size of its output capacitor (due to the pulsating current). At low-output voltages, the PRC is preferable due to its output inductor; at high output voltages the DRC-PRC is preferable because of its output capacitor. The difference between the PRC and DRC-PRC conduction losses is not clearly significant due to the approximation used in determining these. (Only the peak tank current was available, the rms tank current was estimated as 71 percent of the peak.)

The five dc-dc converter designs of Table 5.1 are all therefore considered suitable for high power use. The choices among them depend on the conduction loss/switching loss tradeoff for the available switching devices, as well as the possible incorporation of unavoidable parasitics into the resonant topologies.



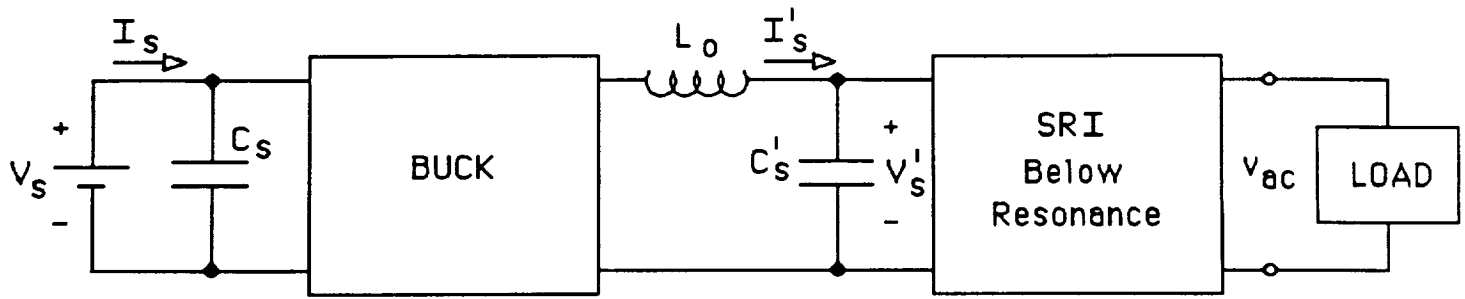
## DC-AC INVERTERS

### Comparison of Four Topologies

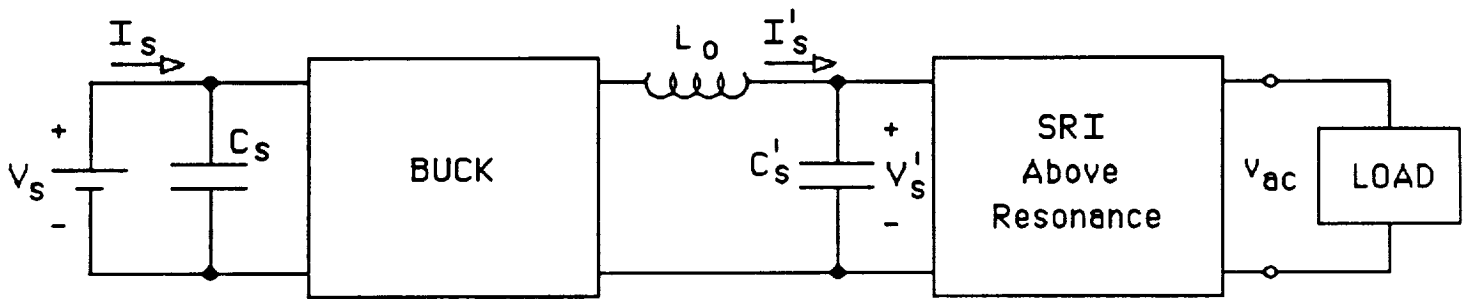
If an ac transmission and distribution system is selected, a dc-ac inverter will be required at the source. This comparison assumes a two-to-one dc source voltage variation ( $K_{TD} = 2$ ) and constant frequency ac output. Fig. 5.1 shows four possible source-converter systems, each a compound of two converters. These four topologies are compared based on the following assumptions:  $K_{TD} = 2$ , 5 percent ripple on voltage-interfacing capacitors and 10 percent ripple on current-interfacing inductors (at full-load current levels). Four ohmic switching devices are assumed for each converter, a total of eight. They are all assumed to follow the model  $R_{DS} = K V^{2.5}$  and have identical area factors "K"; however, the two converters may be equipped with sets having different  $R_{DS} - V$  tradeoffs.

One transformer is assumed for the first three systems of Fig. 5.1 (a, b and c); it might be associated with either of the two converters. The last case, Fig. 5.1(d), the PC-PRI, requires two transformers if full-bridge inverters are used.

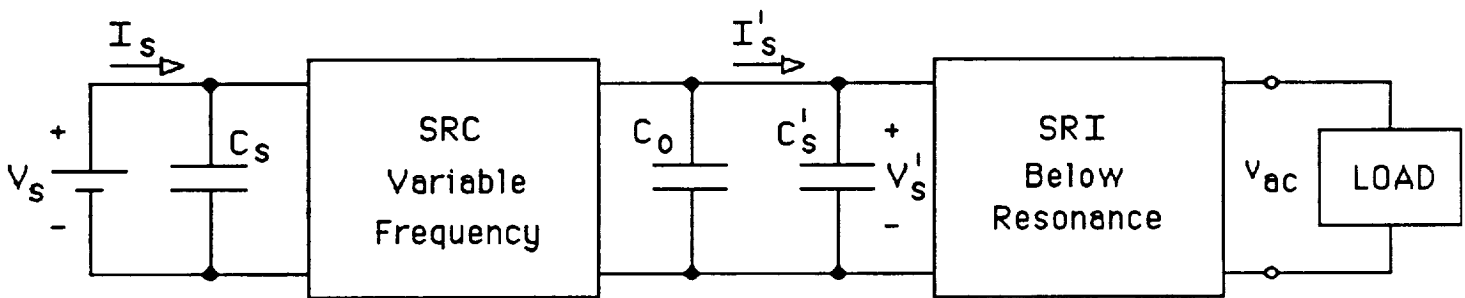
The use of two transformers, one associated with each converter, provides some useful options. First of all, the voltage/current levels in the second converter can be scaled to the optimum values for the switching devices and other components. Secondly, two transformers provide additional control over EMI by breaking possible ground loops and attenuating the propagation of noise in the common mode.



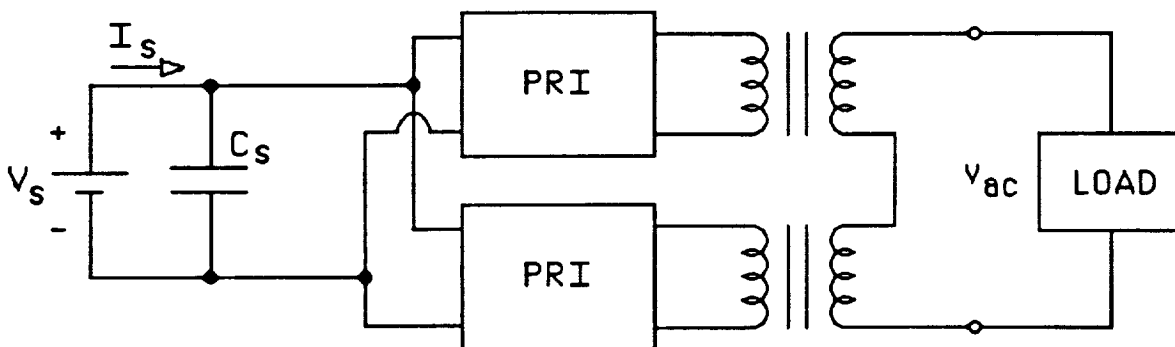
(a) Buck/Fixed-Frequency SRI, Below Resonance



(b) Buck/Fixed-Frequency SRI, Above Resonance



(c) Variable-Frequency SRC/Fixed-Frequency SRI, Below Resonance



(d) Phase-Controlled PRI

Fig. 5.1 Four fixed-frequency ac distribution systems.

Table 5.1 DC-DC Converter Designs for KTD = 2

	Conduction Loss $\frac{P_{COND}}{P_{DES}}$	Transformer VSI Ampere Product $VSI \cdot \Sigma ni$	Interface-Stored Energy	Tank-Stored Energy
Buck	$3I_s(max) K V_s^{1.5}(max)$	$6.3 \frac{P_{DES}}{\omega}$	$15.0 \frac{P_{DES}}{\omega}$	-----
SRC- Below Resonance	$6.9 I_s(max) K V_s^{1.5}(max)$	$12.3 \frac{P_{DES}}{\omega_{max}}$	$18.4 \frac{P_{DES}}{\omega_{max}}$	$8.3 \frac{P_{DES}}{\omega_{max}}$
SRC- Above Resonance	$8.6 I_s(max) K V_s^{1.5}(max)$	$7.0 \frac{P_{DES}}{\omega_{min}}$	$18.4 \frac{P_{DES}}{\omega_{min}}$	$0.58 \frac{P_{DES}}{\omega_{min}}$
PRC- Current-Sourced Rectifier	$8.8 I_s(max) K V_s^{1.5}(max)$	$6.3 \frac{P_{DES}}{\omega_{min}}$	$21.8 \frac{P_{DES}}{\omega_{min}}$	$2.9 \frac{P_{DES}}{\omega_{min}}$
PRC- Discontinuous- Rectifier Conduction	$11.5 I_s(max) K V_s^{1.5}(max)$	$7.2 \frac{P_{DES}}{\omega_{min}}$	$32.0 \frac{P_{DES}}{\omega_{min}}$	$1.3 \frac{P_{DES}}{\omega_{min}}$

The four topologies of Fig. 5.1 are compared in Table 5.2 in terms of conduction loss, transformer volt-second-ampere product, energy stored in the interface components shown in Fig. 5.1, and the energy stored in the resonant tank(s). Figs. 5.1(a) and 5.1(b) show the combination of the buck converter with the SRI, operating below and above resonance, respectively. Estimated total ohmic-device conduction losses for each converter are shown in Table 5.2. Because the first converter may contain a transformer, the voltage/current levels in the second converter could be quite different. Transformer size requirements for each converter are indicated; however, only one is essential. The interface-stored energy for the second SRI includes only its input capacitor.

In all cases, the cost of the load rectifier-filter is not included in this comparison. Tank-stored energy at full-load, and with the load short-circuited, is indicated. It should be noted that tank energy in the second converter increases during a load fault because it is driven at constant frequency. This increase is a transient lasting until the interstage capacitor is discharged.

The third possibility, Fig. 5.1(c), uses two series-resonant converters, and thus provides switching loss reduction in exchange for increased conduction losses. It is evident that above-resonance operation of the SRC generally provides lower stored energy in the resonant tank, and should therefore be selected if zero-current device turn-off is not required.

However, it was shown in the previous chapter that the below-resonance approach tends to limit the peak switch currents under fault conditions to substantially lower levels than the above-resonance design. The increased stored-energy is probably a good price to pay for this benefit. The output-side SRI should probably be operated below resonance, therefore. The input-side converter could be either a buck converter or a SRC operated above resonance.

The fourth possibility considered is that of the phase-controlled PRI of Fig. 5.1(d). This inverter provides a low-distortion sinusoidal output voltage (as opposed to the trapezoidal voltage waveform of the SRI). The price paid for this benefit is seen in the greater stored energy ratings of its resonant tanks. However, it must be pointed out that the amount of energy indicated is not necessarily stored under any one set of conditions, but is the sum of the worst-case ratings of all six tank elements. The fact that both of the constituent inverters and their input filter must support the line voltage, assumed here to be as high as twice low-line, accounts for the high predicted conduction losses and interface-stored energy.

If no line voltage regulation were necessary, the conduction loss of the PC-PRI would be comparable to that of the SRI. Another notable disadvantage of the PRI is the high total transformer rating. Again, this is due to the assumed source voltage turn-down ratio, because each transformer is exposed to a voltage proportional to the source voltage. A half-bridge version [34] of the PC-PRI combines the outputs of the two unit inverters prior to a single transformer, and thus requires a transformer half as big, but at the cost of twice the rms current in twice as many input voltage-sourcing capacitors.

Table 5.2 DC-AC Inverter Designs for KTD = 2

	Conduction Loss $\frac{P_{COND}}{P_{DES}}$	Transformer VSI Ampere Product $V_{SI} \cdot \Sigma n_i$	Interface-Stored Energy	Tank-Stored Energy	Tank Stored Energy (Load Fault)
Buck/SRI, Below Resonance  Fig. 5.1(a)	$3I_s(\max)K V_s^{1.5}(\max)$ + $4.1I_s' K (V_s')^{1.5}$	$6.3 \frac{P_{DES}}{\omega_{BUCK}}$ or $7.4 \frac{P_{DES}}{\omega_{AC}}$	$15.0 \frac{P_{DES}}{\omega_{BUCK}}$ + $3.7 \frac{P_{DES}}{\omega_{AC}}$	$4.4 \frac{P_{DES}}{\omega_{AC}}$	x $9.0 \frac{P_{DES}}{\omega_{AC}}$
Buck/SRI, Above Resonance  Fig. 5.1(b)	$3I_s(\max)K V_s^{1.5}(\max)$ + $6.2 I_s' K (V_s')^{1.5}$	$6.3 \frac{P_{DES}}{\omega_{BUCK}}$ or $7.0 \frac{P_{DES}}{\omega_{AC}}$	$15.0 \frac{P_{DES}}{\omega_{BUCK}}$ + $3.7 \frac{P_{DES}}{\omega_{AC}}$	$1.2 \frac{P_{DES}}{\omega_{AC}}$	x $5.4 \frac{P_{DES}}{\omega_{AC}}$
SRC/SRI, both below resonance  Fig. 5.1(c)	$6.9I_s(\max)K V_s^{1.5}(\max)$ + $4.1I_s' K (V_s')^{1.5}$	$12.3 \frac{P_{DES}}{\omega_{SRC}}$ or $7.4 \frac{P_{DES}}{\omega_{AC}}$	$18.4 \frac{P_{DES}}{\omega_{SRC}}$ + $3.7 \frac{P_{DES}}{\omega_{AC}}$	$10.0 \frac{P_{DES}}{\omega_{SRC}}$ + $4.4 \frac{P_{DES}}{\omega_{AC}}$	<10.0 $\frac{P_{DES}}{\omega_{SRC}}$ + $9.0 \frac{P_{DES}}{\omega_{AC}}$
PC-PRI $\omega_o = \frac{\omega}{0.65}$ Fig. 5.1(d)	$24.7I_s(\max)K V_s^{1.5}(\max)$	$11.3 \frac{S_{DES}}{\omega_{AC}}$ (sum of two)	$44.1 \frac{S_{DES}}{\omega_{AC}}$	$17.2 \frac{S_{DES}}{\omega_{AC}}$	$17.2 \frac{S_{DES}}{\omega_{AC}}$

\*Sum of the component ratings, all do not maximize under same conditions

xOccurs on a transient basis as interstage filter capacitor discharges

All candidates on Table 5.2 are viable. The choice of the input stage converter is a tradeoff between conduction losses and switching losses. Either a buck converter or an above-resonance SRC is recommended, with a below-resonance SRC a good choice if zero-current switching is required. The use of a SRI output inverter operating below-resonance is recommended. The two-stage approach works better when large source-voltage turn-down ratios are required. The PC-PRI is more costly in terms of conduction losses and transformer size, the difference increasing with the turn-down ratio requirement.

### **Additional Topologies**

Two additional dc-ac inverter topologies might be considered; these are combinations of pulse-width modulation with parallel-loaded resonant inverters. One is the PWM-PRI [33] discussed previously. The other is the TRW resonant converter [18], also discussed previously. The latter is similar to the former, except that the TRW approach places the resonant inductor in the dc link between a buck converter and the resonant inverter. The approach of [33] drives the resonant tank from a pulse-width modulated switching matrix. It is possible that these approaches will be competitive with the systems on Table 5.2 which include a buck converter. Neither of these two is sufficiently described to allow a detailed comparison without extensive analytical work. It does seem that both will have switching losses, but would establish a low-distortion ac output.



### **Additional Considerations**

There are some additional considerations to be made in selecting the source inverter for an ac system. These include the voltage/current waveform requirements and surviveability of load faults (including all conceivable transient conditions). In the first case there is a choice to be made between the quasi-square-wave voltage/quasi-sinusoidal current characterizing the SRI-based approach considered here and the low-distortion voltage and current of the PC-PRI as considered here. The second issue involves the thorough testing by simulation and experiment of the implications of all possible load faults under transient conditions.

The load rectifiers required by each system also need to be considered. The SRI-based systems have thus far assumed simple voltage-sourced rectifiers, which are the cause of the non-sinusoidal system voltage. The PC-PRI system has been predicated on more-complex rectifiers which produce sinusoidal input current. These will require resonant tanks with their attendant stored energy and losses.

It seems apparent that the waveforms appearing at the loads are basically unimportant to the loads. The effects of large voltage or current harmonics on the distribution system is another issue. A SRI-based system having a length of high-capacitance (low voltage-drop) cable was successfully demonstrated [11]. However, it still seems possible that given a large enough distribution system and harmonic content at a high enough frequency, resonance in the distribution system could conceivably be excited. This issue should be studied upon adoption of an SRI-based system.

The PC-PRI approach generally includes the assumption that the major load rectifiers will have low harmonic content. This means substantially more complex rectifiers are needed for this system, a cost which should be charged against it in any comparison. However, if low distortion is determined to be necessary, then special rectifiers could also be used with a SRI, a possibility which has not yet been investigated.

Fault survival is another area in which there is considerable lack of information. All of the topologies considered here will reach a satisfactory steady state for any short- or open-circuit fault. However, the fault transient should also be considered. For example, the PC-PRI was studied during application and removal of an ac-side short-circuit, with the result that there was a transient reversal of the expected commutation sequence. This caused no difficulty for a 2500 VA MOSFET-based laboratory inverter; thus it was "fault proof." The same inverter built with thyristors would have had a commutation failure. This commutation-sequence reversal was easily dealt with at the 2500 VA level, but at higher power levels where slower switching devices would be used, it would possibly compromise the snubber design. A simple solution has been suggested [7] and verified by simulation. No experimental verification has been made, however.

The SRC/SRI system of Fig. 5.1(C) has been tested experimentally [11] for fault survival with good results. The 2500W SRI using IGTs survived repeated faults. However, the switching conditions during the transient were not recorded. This should be studied if the SRC/SRI is adopted for an ac distribution system.

The TRW resonant inverter is also fault-proof, provided the PWM switches can commute their peak currents. Both turn-on and turn-off is required, and in this area it is comparable to the most unfavorable result that could be obtained from the SRC/SRI or PC-PRI approaches. The TRW converter is fault-proof because it does not rely on the resonant tank for low-loss commutation, and in this way is quite comparable to a buck converter/resonant inverter cascade.

## **Recommendations**

Some recommendations are now given for each converter/inverter considered, depending upon the choice of three possible distribution systems: dc, high-distortion ac, or low-distortion ac. If a dc system is chosen, the best converters would be the buck or the SRC, depending upon the conduction and switching loss characteristics of the devices used. The SRC would have approximately two to three times the conduction loss of the buck converter, but it could substantially reduce switching loss. Above-resonance operation of the SRC is definitely preferable because it allows the use of a transformer comparable to that of the buck converter, and significantly smaller tank, slower antiparallel diodes and lossless snubbers.

The below-resonance SRC would have marginally lower conduction loss than the above-resonance SRC, or either PRC considered. The PRC with current-sourced rectifier is probably best used with unusually low output-side voltage levels. The PRC with discontinuous-rectifier conduction is probably best used with unusually high output-side voltage levels, especially if the transformer has significant parasitic capacitance.

The SRC/SRI combination can be effectively used if a high-distortion ac system is chosen. This topology provides the conduction loss/switching loss tradeoff characteristic of the resonant inverters. The output SRI should be operated below-resonance; this provides the most effective load-fault protection for its switching devices for a given tank size. The input SRC can be operated above-resonance to obtain the benefits listed previously. Buck/SRI combinations are also viable, but must be questioned in light of the widespread assumption that ac systems are justified by a need for resonant switching. If ac is adopted for reasons other than resonant switching, then the buck/SRI combination (as well as the PWM-PRC and TRW resonant inverter) should be considered.

The SRC/SRI should be studied to verify satisfactory switching conditions during a load-fault transient, although the laboratory results thus far are encouraging.

The PC-PRI is recommended if the following are found to be bona fide system requirements: (1) a low-distortion ac system, and (2) resonant switching. This inverter will have a high conduction loss relative to the SRC/SRI for a turn-down ratio of two. For higher turn-down ratios, the PC-PRI is increasingly disadvantaged, for a turn-down ratio of unity the difference is not great.

If low-distortion ac is not a requirement, however, it should not be provided, because of this cost of providing it. The PC-PRI has a larger set of transformers than an above-resonance SRC or fixed-frequency SRI; however, its two transformers are together comparable to that of a below-resonance SRC. The PWM-PRI and TRW resonant inverter are also candidates for a low-distortion ac system if resonant switching is not a requirement. These should be studied further if such were the case. However, if resonant switching is not a requirement, it needs to be asked if ac is also.

The PC-PRI has been found to have reversed commutations under fault transient conditions. A suggested remedy has been demonstrated by simulation, but not in hardware.

## VI. SUMMARY

There are two closely linked issues to be dealt with in designing a high-power transmission and distribution system. One is the choice between ac and dc systems on their inherent merits, and the other is the necessity (or lack thereof) of having resonant switching in the power converters. An ac system provides simple voltage scaling through the use of transformers; a dc system is simpler to control. Issues such as efficiency, weight or current interruption do not strongly favor either system. Resonant switching trades switching loss for conduction loss. The available switching devices determine whether this is a good trade or not. The adoption of an ac system implies the use of resonant switching converters.

In light of this, ac inverters which do not assure at least some "easy" commutations (e.g. PWM-PRI or TRW resonant inverter) are of questionable utility. If the provision of resonant commutations is being relied on in the choice of switching devices and snubber design, then all possible fault transients should be closely studied for any chosen inverter topology. If commutation reversals are not a concern, then the same switching devices could be used to build a simpler dc-dc converter which would have lower conduction losses (albeit higher switching losses).

If a dc system is chosen, the buck converter and the SRC provide two good alternatives. Above-resonance operation of the SRC provides a lower weight design if the switching devices permit. The full-bridge topology is generally most favorable: It avoids the capacitor penalty of the half-bridge and the transformer penalty of the push-pull.

If resonant switching is considered critical, then an ac system might be considered. The fixed-frequency below-resonance SRI provides a good ac-system source converter if high distortion is acceptable. This will depend on whether a distribution system free of excessive parasitic resonances can be constructed. The compatibility of

the SRI switching devices and their snubbers with the commutations occurring during a load fault transient should be studied in detail.

If low distortion is required, then the PC-PRI is recommended, although it will have higher conduction losses than the SRC/SRI cascade when a large source voltage range is required. Alternatives which provide low distortion ac without low-loss commutation of their switches do not seem useful, but rather suggest the use of dc instead. It must be kept in mind that a low distortion ac system will require low-harmonic-current rectifiers at the major loads, an additional loss and weight to be charged against such a system. The PC-PRI has been shown experimentally to have a potential commutation sequence reversal during a load fault, a problem that should be addressed in any high-power design.

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